Compal Confidential

Buffalo KAVAA

LA-5121P Schematics Document

Intel Diamondville Processor/ Calistoga(945GSE)/ ICH7M

2009-03-10

REV: 1.0

Security Classification	Compal Secret Data		
Issued Date	2008/11/17	Deciphered Date	2009/11/17

Compal Electronics, Inc.		
Title: Cover Page		
Size: Custom	Document Number: KAVAA LA-5121P M/B	Rev: 1.0
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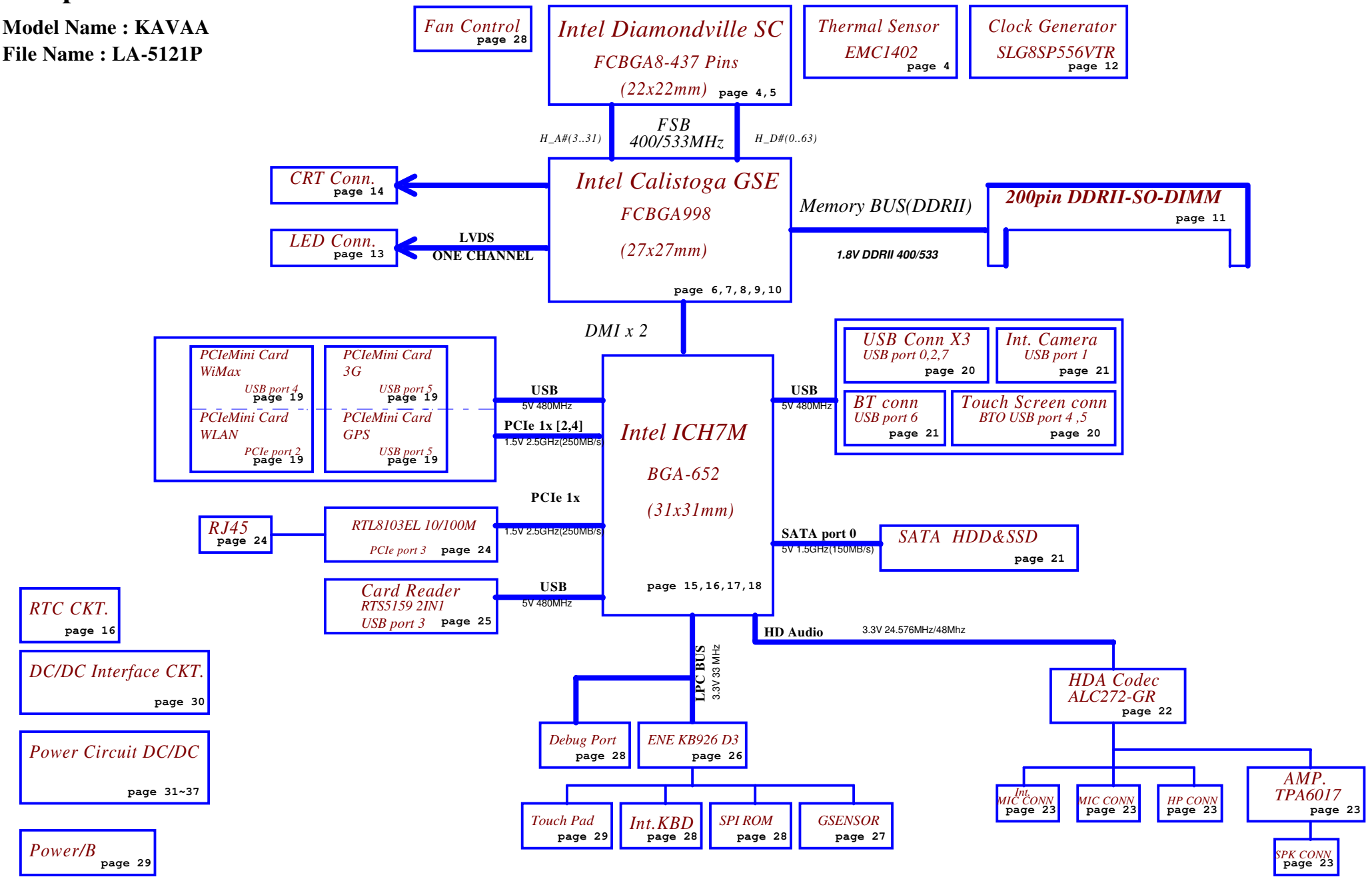
Model Name : KAVAA
File Name : LA-5121P



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Title	Block Diagrams	
Size	Document Number	Rev
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Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	VCCP switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3V_SB	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_WLAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	ON	OFF	OFF
+5VALW	5V always on power rail	ON	OFF	ON	OFF
+5V_SB	5V power rail for SB	ON	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF	ON
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

Function	Mini PCI-E SLOT				CAMERA & MIC		BLUE TOOTH	STAR	G-SENSOR
description									
explain	Wi-Fi	WiMax	3GGPS	3G	CAMERA	MIC	BLUE TOOTH	POWER SAVING	HDD PROTECT
BTO	WLAN@	WIMAX@	3GGPS@	3G@	CAM@	MIC@	BT@	STAR@	GSENSOR@

Function			
description			
explain			
BTO			

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
EMC1402	1001 010X b

ICH7M SM Bus address

Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb

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Title: Notes List

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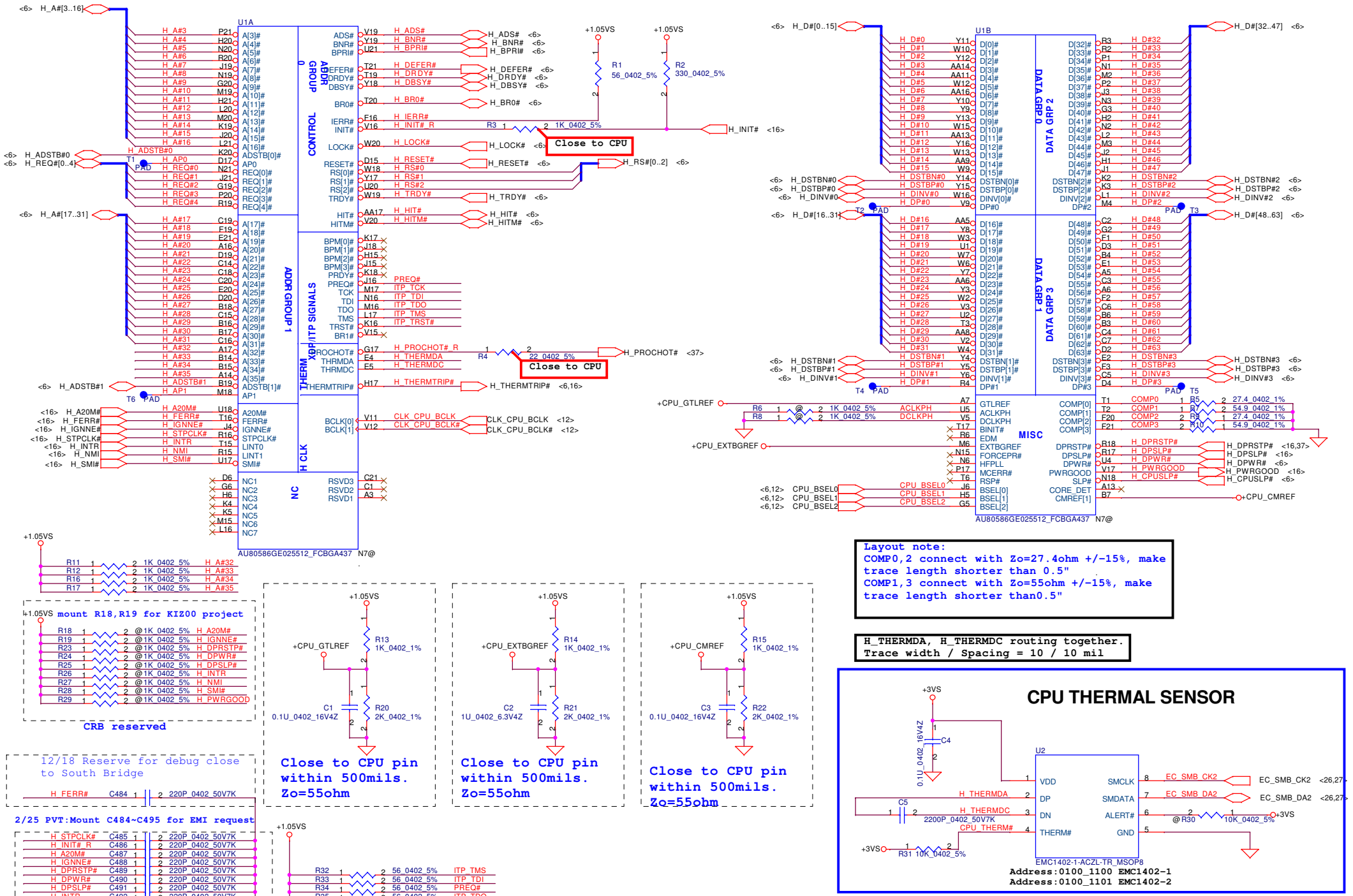

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Compal Electronics, Inc.

Title	Diamondville(1/2)		
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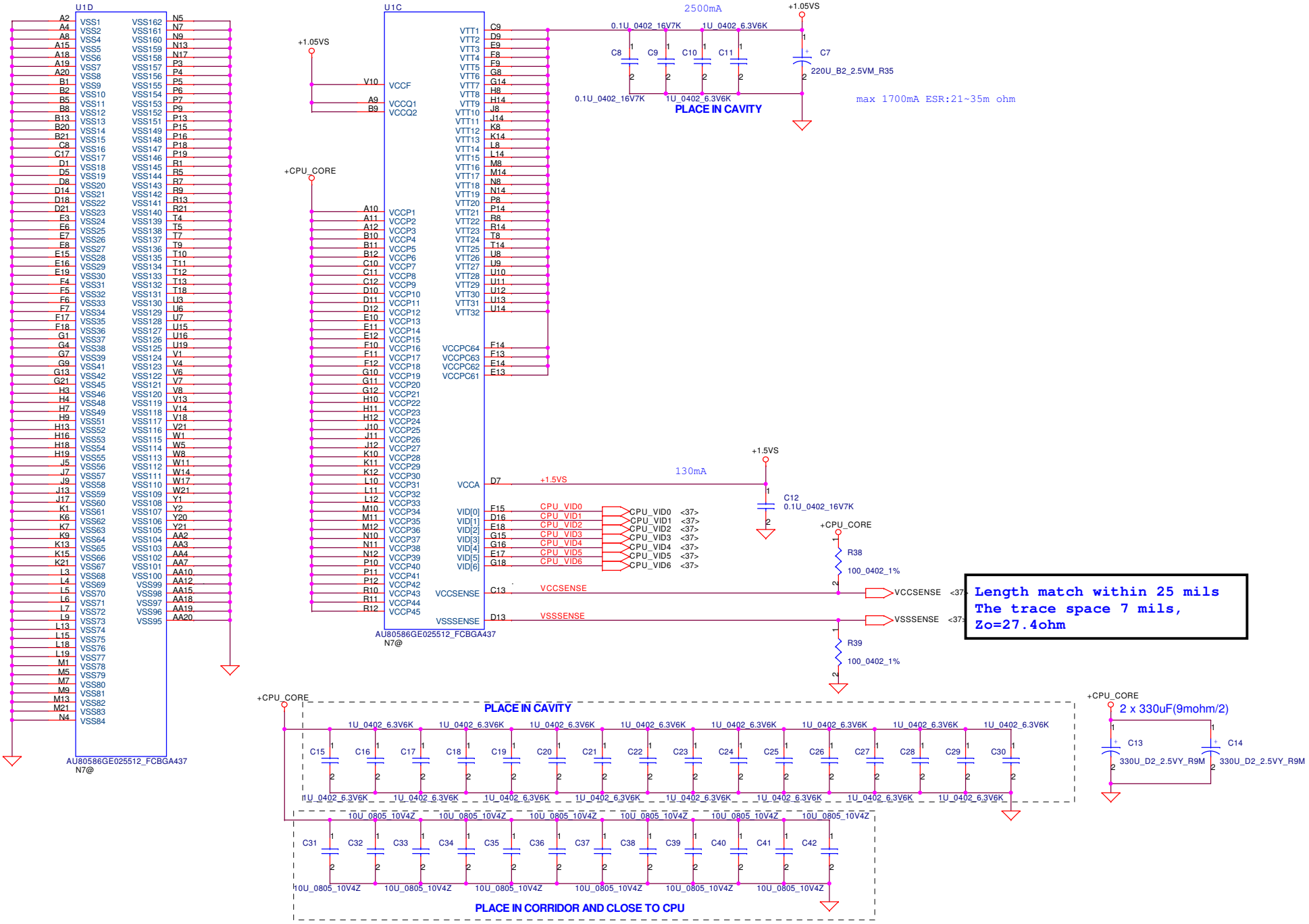

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title	Diamondville(2/2)	
Size: Custom	Document Number: KAVAA LA-5121P M/B	Rev: 1.0
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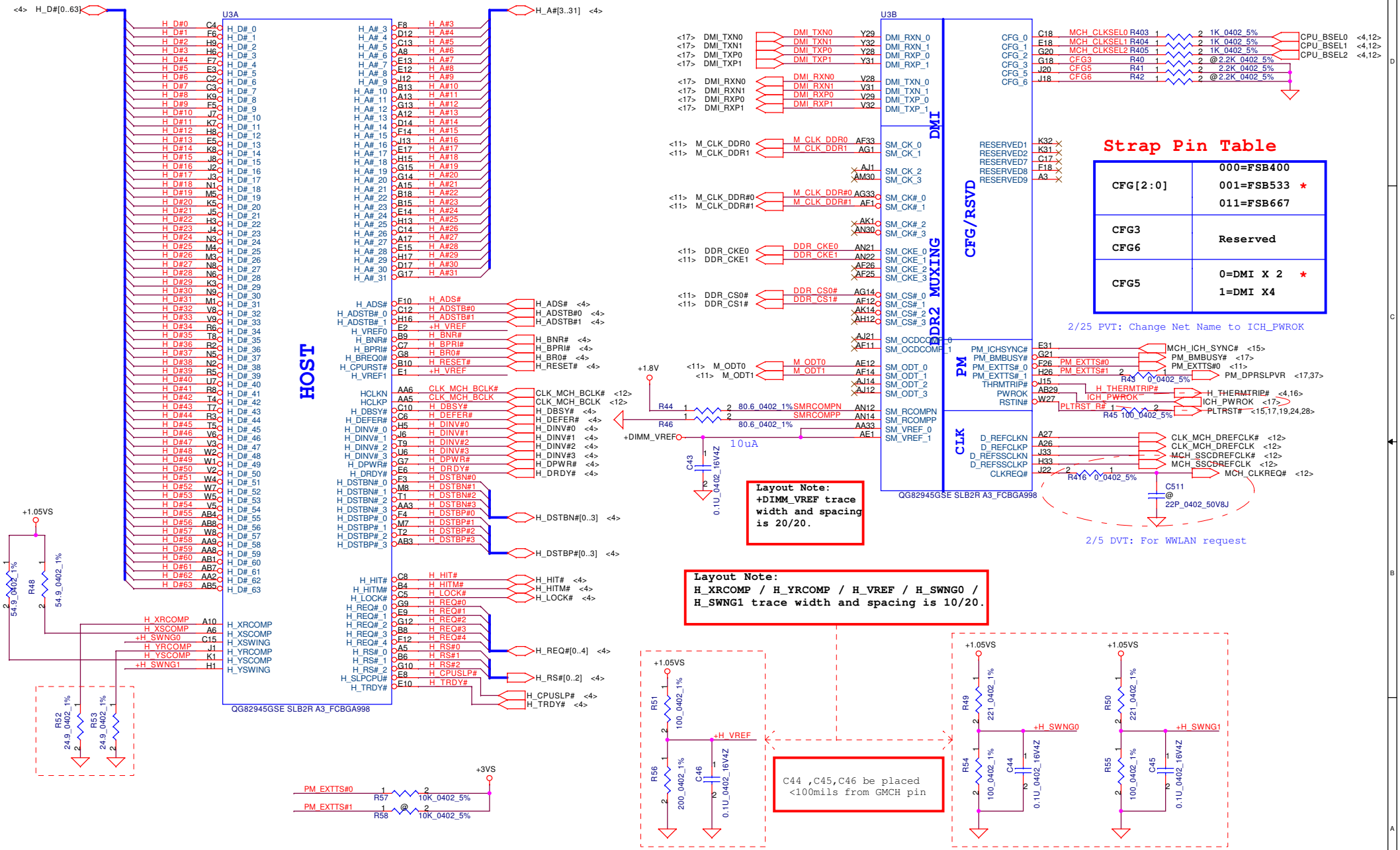

Security Classification	Compal Secret Data		
Issued Date	2008/11/17	Deciphered Date	2009/11/17

Compal Electronics, Inc.

Title: Calistoga(1/5)-GTL/DMI/DDR

Size	Document Number	Rev
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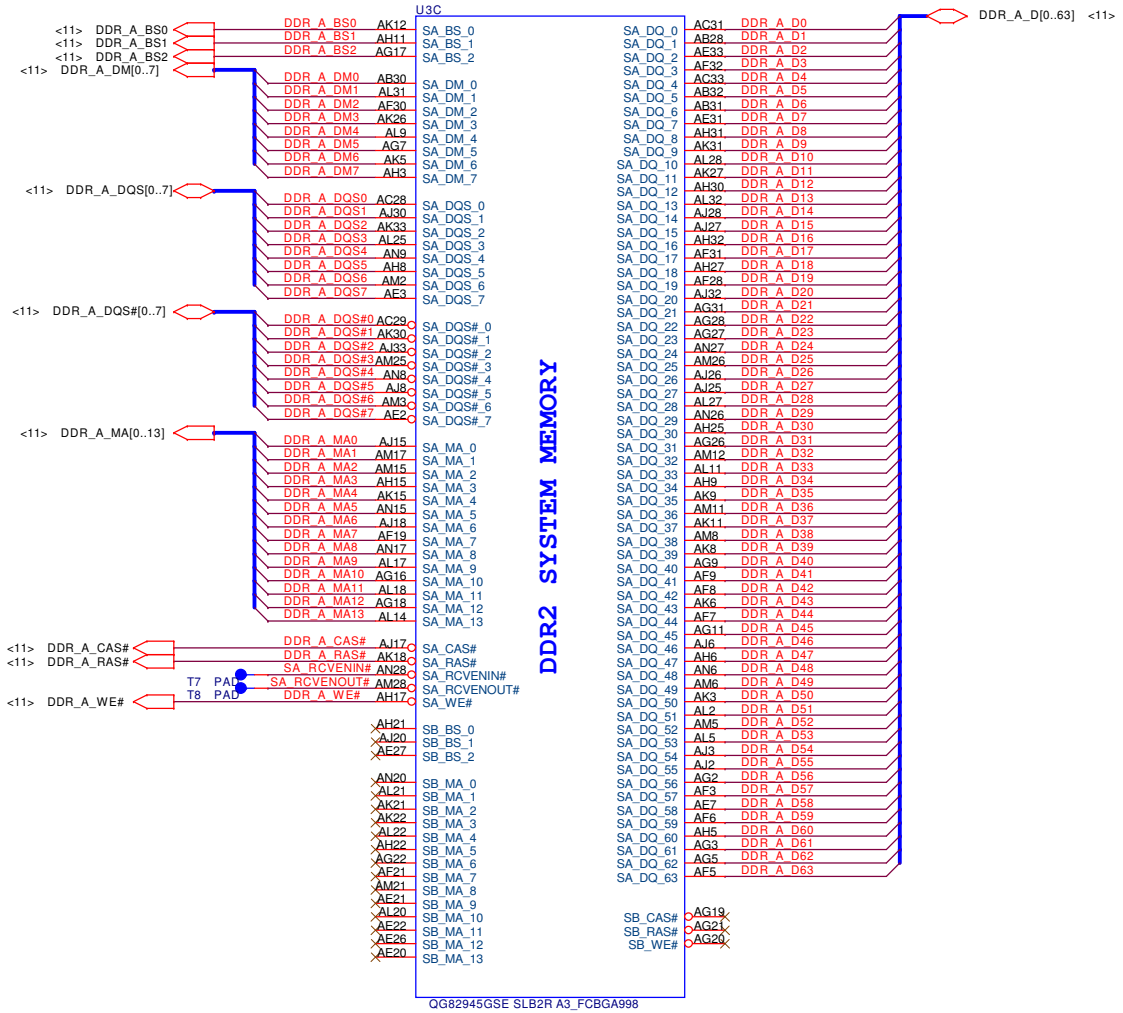

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: Calistoga(2/5)-DDR2

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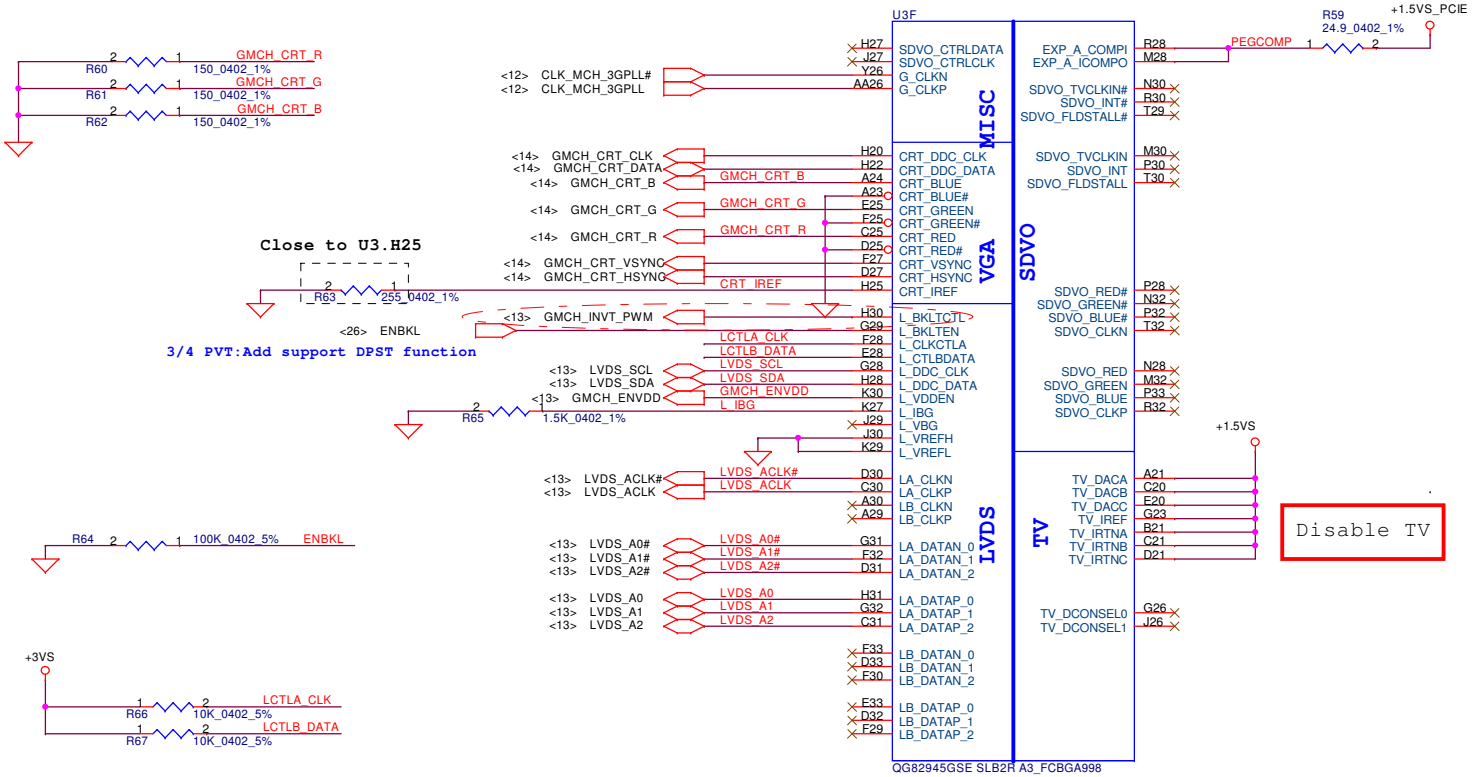

Security Classification	Compal Secret Data		
Issued Date	2008/11/17	Deciphered Date	2009/11/17

Compal Electronics, Inc.

Title: Calistoga(3/5)-VGA/LVDS/TV

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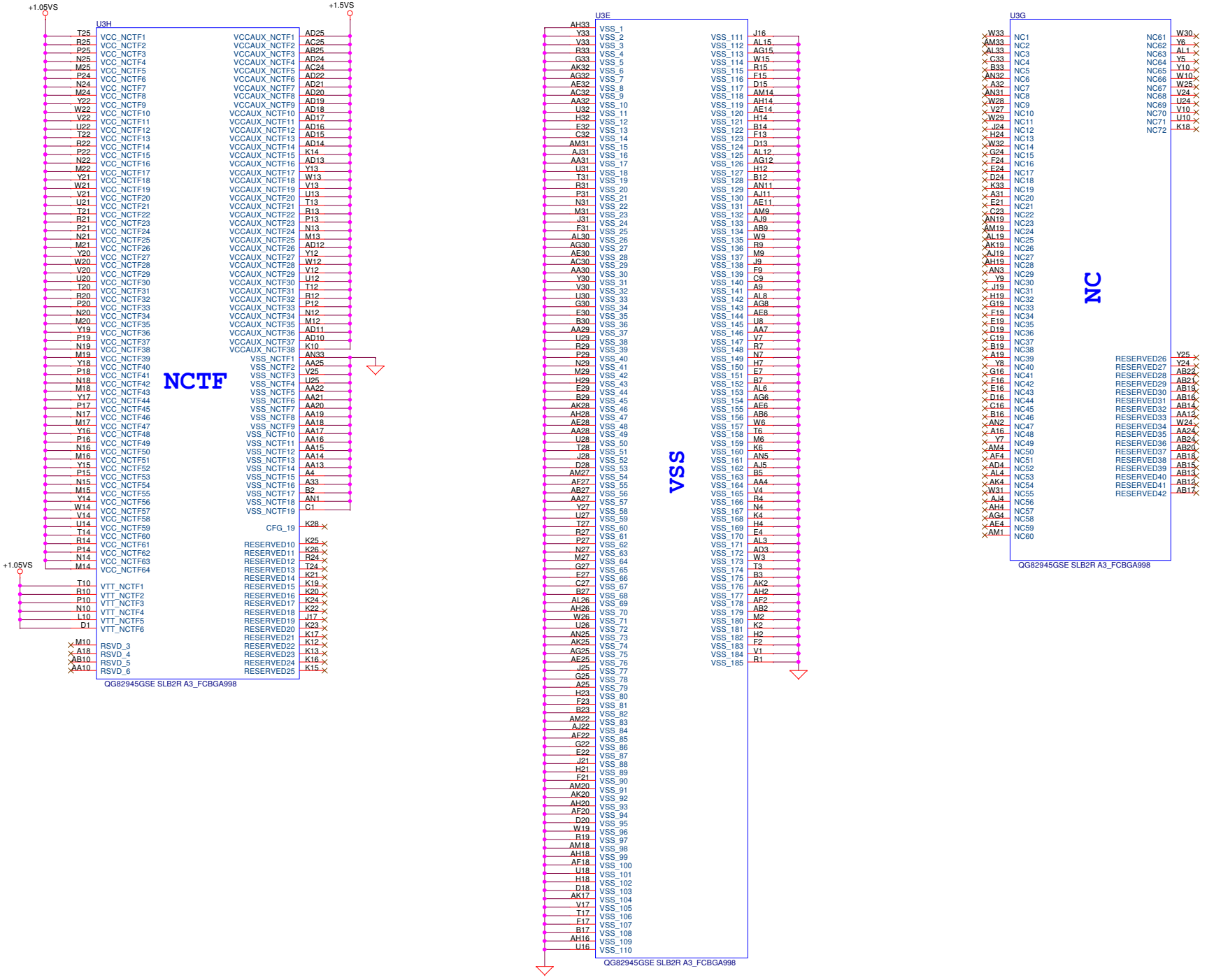

Security Classification	Compal Secret Data		
Issued Date	2008/11/17	Deciphered Date	2009/11/17

Compal Electronics, Inc.

Title: Calistoga(4/5)-PWR/GND

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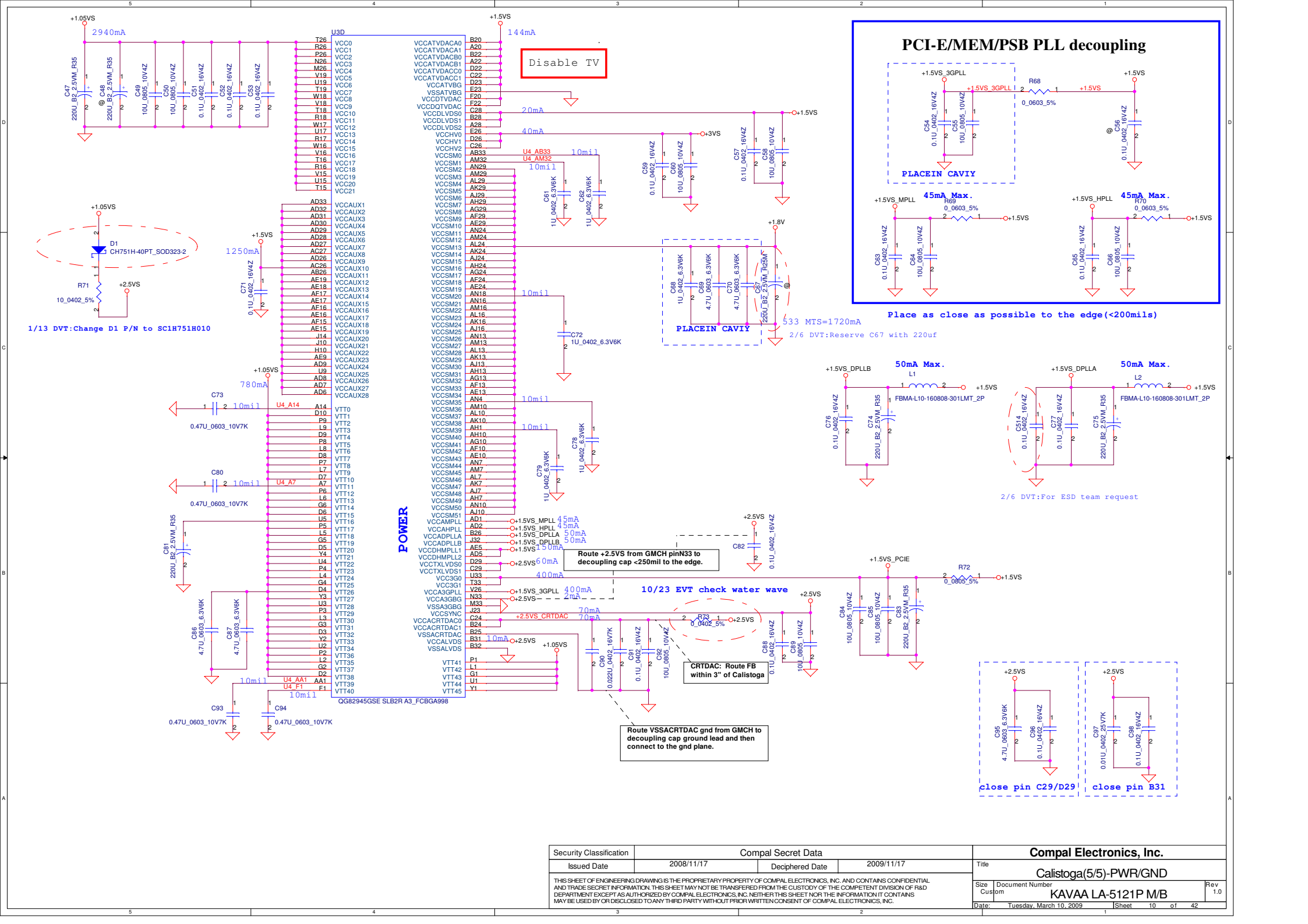

Security Classification	Compal Secret Data		
Issued Date	2008/11/17	Deciphered Date	2009/11/17

Compal Electronics, Inc.

Title: Calistoga(5/5)-PWR/GND

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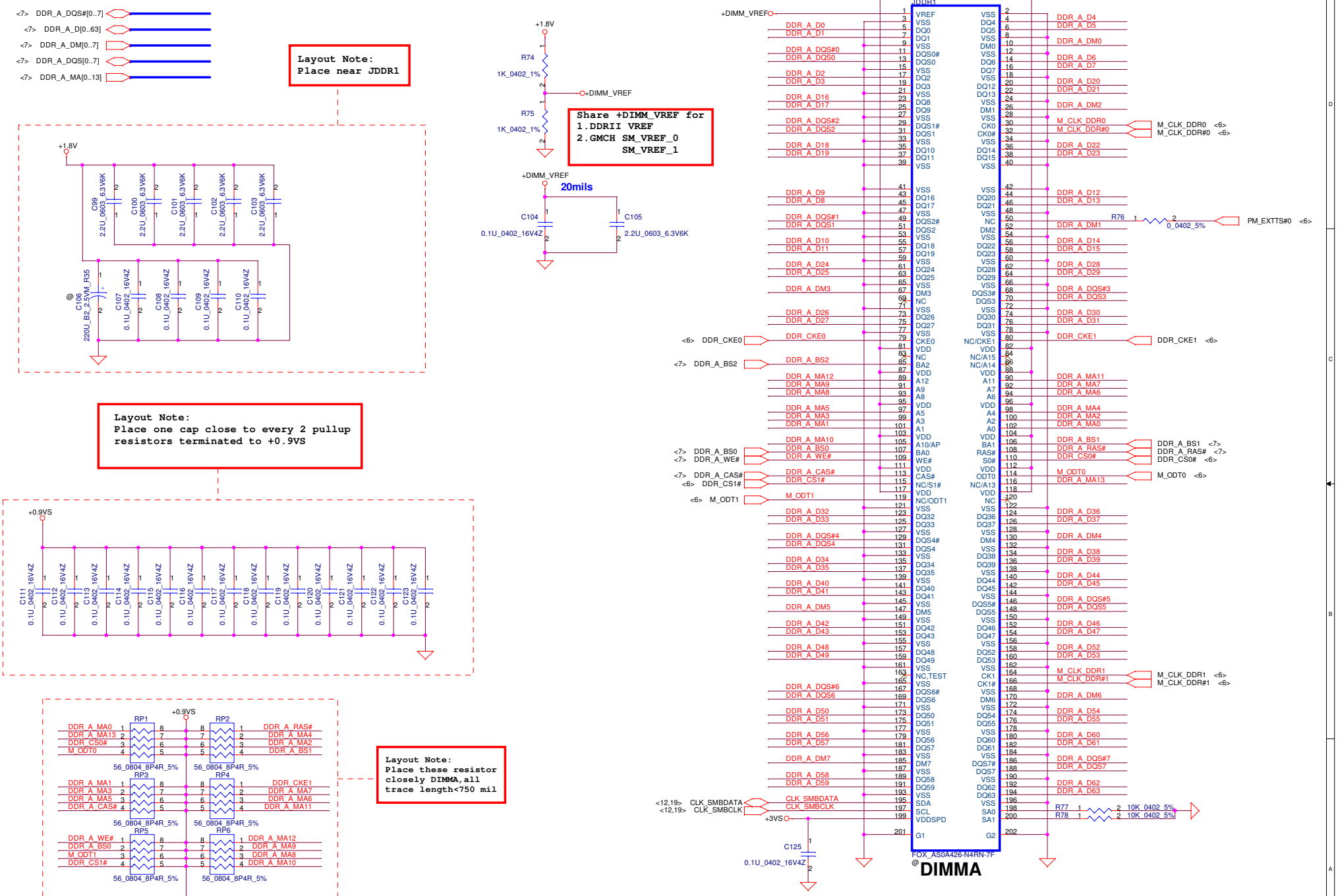

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Compal Electronics, Inc.

Title: DDRII-SODIMMA

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FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

+3VM_CK505 250 mA

R81 FBMH1608HM601-T_0603 For WWAN request

C126 10U_0805_10V4Z; C127–C132 0.1U_0402_16V4Z; C133 47P_0402_50V8J

+1.05VM_CK505 80 mA

R82 FBMH1608HM601-T_0603

C134 10U_0805_10V4Z; C135–C140 0.1U_0402_16V4Z; C141 47P_0402_50V8J

For WWAN request

2/25 PVT:Change R81,R82 form 0 ohm to FBMH1608HM601

2/25 PVT:Mount C133,C141 with 47P

+3VS R83 2.2K_0402_5% R84 2.2K_0402_5%

Q1A 2N7002DW-T/R7_SOT363-6

<17> ICH_SMBDATA — CLK_SMBDATA

Q1B 2N7002DW-T/R7_SOT363-6

<17> ICH_SMBCLK — CLK_SMBCLK

SA000020K00 (Silego : SLG8SP556VTR)

SA000020H10 (ICS : ICS9LPRS387AKLFT)

2/5 DVT: Reserve C509,C510 with 10P

U4 SLG8SP556VTR_QFN72_10X10

+3VM_CK505: VDD_SRC (55), VDD_REF (6), VDD_PCI (12), VDD_CPU (72), VDD_48 (19), VDD_PLL3 (27)

+1.05VM_CK505: VDD_CPU_IO (66), VDD_PLL3_IO (31), VDD_SRC_IO (62), VDD_SRC_IO (52), VDD_IO (23), VDD_SRC_IO (38)

VSS_PCI (18), VSS_REF (3), VSS_48 (22), VSS_IO (26), VSS_CPU (69), VSS_PLL3 (30), VSS_SRC (34), VSS_SRC (59), VSS_SRC (42), VSS (73)

Pin	Signal	Destination
9	SDA	CLK_SMBDATA <11,19>
10	SCL	CLK_SMBCLK <11,19>
71	CPU_0	CLK_CPU_BCLK <4>
70	CPU_0#	CLK_CPU_BCLK# <4>
68	CPU_1	CLK_MCH_BCLK <6>
67	CPU_1#	CLK_MCH_BCLK# <6>
24	SRC_0/DOT_96	CLK_MCH_DREFCLK <6>
25	SRC_0#/DOT_96#	CLK_MCH_DREFCLK# <6>
28	LCDCLK/27M	MCH_SSCDREFCLK <6>
29	LCDCLK#/27M_SS	MCH_SSCDREFCLK# <6>
32	SRC_2	CLK_MCH_3GPLL <8>
33	SRC_2#	CLK_MCH_3GPLL# <8>
35	SRC_3	CLK_PCIE_SATA <16>
36	SRC_3#	CLK_PCIE_SATA# <16>
39	SRC_4	CLK_PCIE_WWAN <19>
40	SRC_4#	CLK_PCIE_WWAN# <19>
57	SRC_6	CLK_PCIE_WLAN <19>
56	SRC_6#	CLK_PCIE_WLAN# <19>
61	SRC_7	
60	SRC_7#	
64	SRC_8/CPU_ITP	
63	SRC_8#/CPU_ITP#	
44	SRC_9	CLK_PCIE_LAN <24>
45	SRC_9#	CLK_PCIE_LAN# <24>
50	SRC_10	CLK_PCIE_ICH <17>
51	SRC_10#	CLK_PCIE_ICH# <17>
48	SRC_11	
47	SRC_11#	
37	CLKREQ_3#	SATA_CLKREQ# <17>
41	CLKREQ_4#	WWAN_CLKREQ# <19>
58	CLKREQ_6#	WLAN_CLKREQ# <19>
65	CLKREQ_7#	
43	CLKREQ_9#	LAN_CLKREQ# <24>
49	SLKREQ_10#	
46	CLKREQ_11#	
21	USB_1/CLKREQ_A#	MCH_CLKREQ# <6>

2/25 PVT:Mount C142,C143,C868 with 22P

CLK_48M_CR and CLK_ICH_48M need to same lengh

For WWAN request: C142 22P_0402_50V8J; R90 22_0402_5% <25> CLK_48M_CR

R91 22_0402_5% <17> CLK_ICH_48M

C143 22P_0402_50V8J; R93 33_0402_5% <17> CLK_ICH_14M

For WWAN request: C868 22P_0402_50V8J

Pin	Signal	Destination
20	USB_0/FS_A	FSA
2	FS_B/TEST_MODE	CPU_BSEL1
7	REF_0/FS_C/TEST_	FSC
8	REF_1	
1	CKPWRGD/PD#	VGATE <17,26,37>
11	NC	
53	CPU_STOP#	H_STP_CPU# <17>
54	PCI_STOP#	H_STP_PCI# <17>
5	XTAL_IN	CLK_XTAL_IN
4	XTAL_OUT	CLK_XTAL_OUT
13	PCI_1	CLK_PCI_DDR_R <28> (R103 33_0402_5%)
14	PCI_2	PCI2_TME
15	PCI_3	
16	PCI_4/SEL_LCDCL	PCI4_SEL <26> CLK_PCI_LPC (R107 33_0402_5%)
17	PCIF_5/ITP_EN	ITP_EN <15> CLK_PCI_ICH (R108 33_0402_5%)

<4,6> CPU_BSEL0 — R86 2.2K_0402_5% — FSA

<4,6> CPU_BSEL1 — CPU_BSEL1

<4,6> CPU_BSEL2 — R104 10K_0402_5% — FSC

+3VS R428 10K_0402_5% H_STP_PCI#_R

3/5 PVT:Reserve R427 with 0 ohm

3/5 PVT:Add R428 with 10Kohm to +3VS

For WWAN request

2/25 PVT:Mount C144,C145,C146 with 22P

For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#

For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS

For PCI2_TME:0=Overclocking of CPU and SRC allowed
(ICS only) 1=Overclocking of CPU and SRC NOT allowed

C147 22P_0402_50V8J — CLK_XTAL_IN

Y1 14.31818MHZ_16PF_DSX840GA

C148 22P_0402_50V8J — CLK_XTAL_OUT

Routing the trace at least 10mil

+3VS

R112 10K_0402_5% PCI2_TME

R113 10K_0402_5% ITP_EN

R114 10K_0402_5% PCI4_SEL

@R115 10K_0402_5%

SRC PORT LIST

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	PCIE_3GPLL
SRC3	PCIE_SATA
SRC4	PCIE_WWAN
SRC6	PCIE_WLAN
SRC7	
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	

+3VS

MCH_CLKREQ# R97 10K_0402_5%

SATA_CLKREQ# R98 10K_0402_5%

WLAN_CLKREQ# R99 10K_0402_5%

WWAN_CLKREQ# R100 10K_0402_5%

LAN_CLKREQ# R101 10K_0402_5%

REQ PORT LIST

PORT	DEVICE
REQ_3#	PCIE_SATA
REQ_4#	PEIC_WWAN
REQ_6#	PEIC_WLAN
REQ_7#	
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	
REQ_A#	MCH_3GPLL

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Compal Electronics, Inc.

Title: Clock Generator CK505

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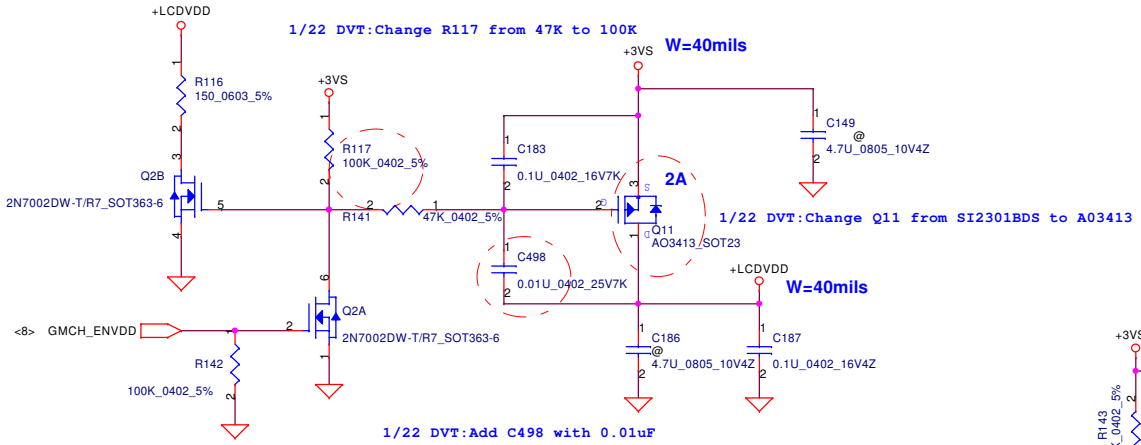
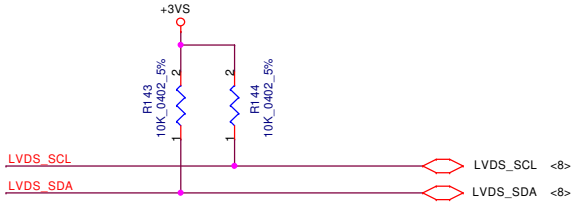
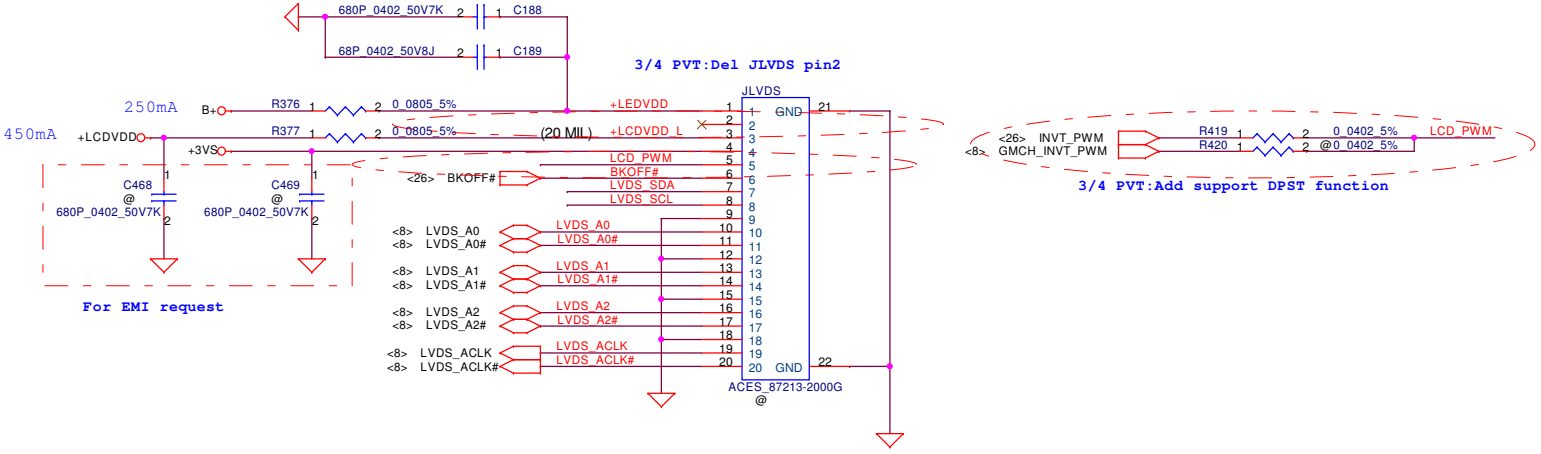
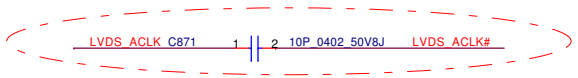
LCD POWER CIRCUIT





LED/PANEL BD. Conn.





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Issued Date	2008/11/17	Deciphered Date	2009/11/17

Compal Electronics, Inc.

Title: LVDS /INVERTER

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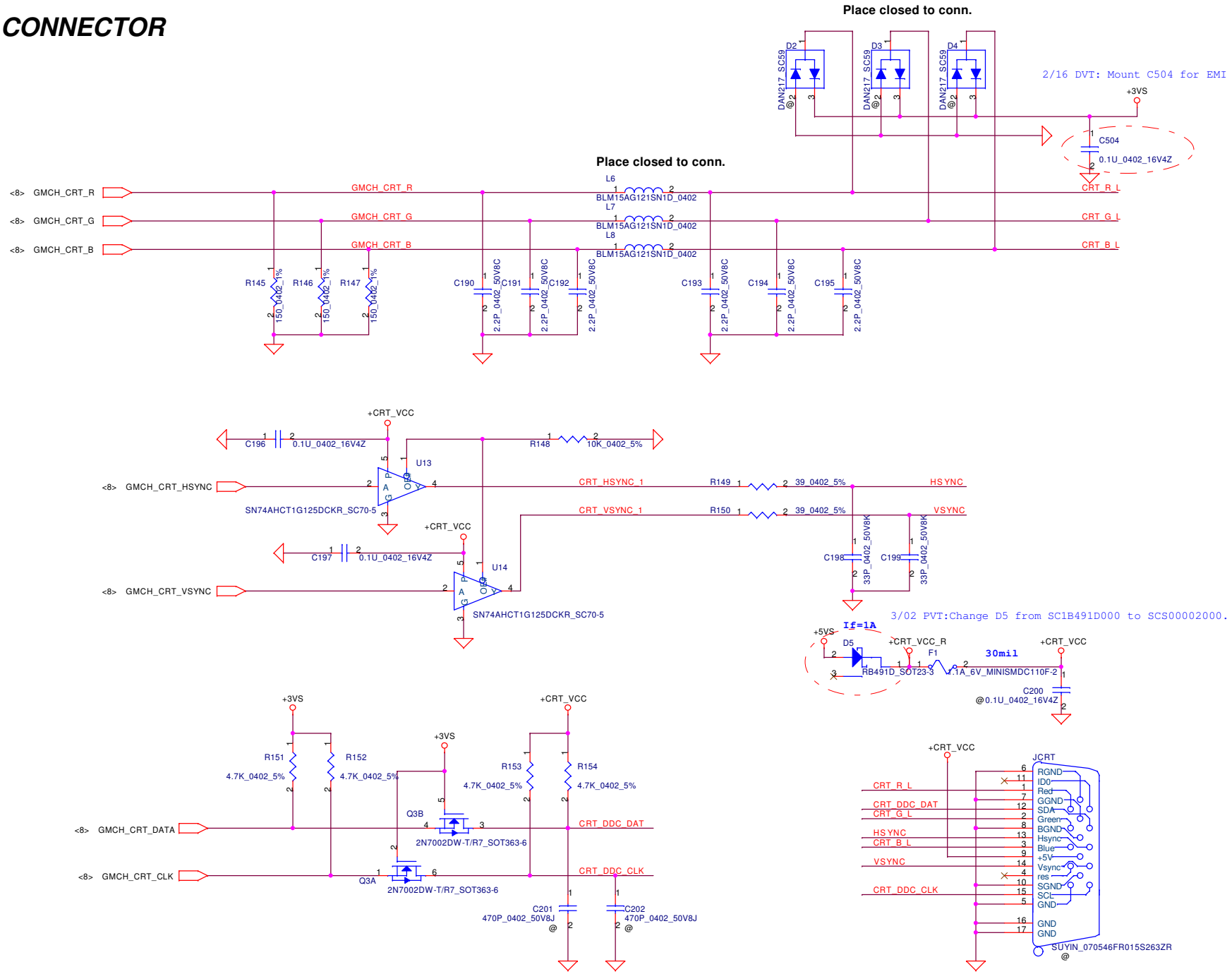
CRT CONNECTOR



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Compal Electronics, Inc.

Title	CRT PORT	
Size	Document Number: KAVAA LA-5121P M/B	Rev: 1.0
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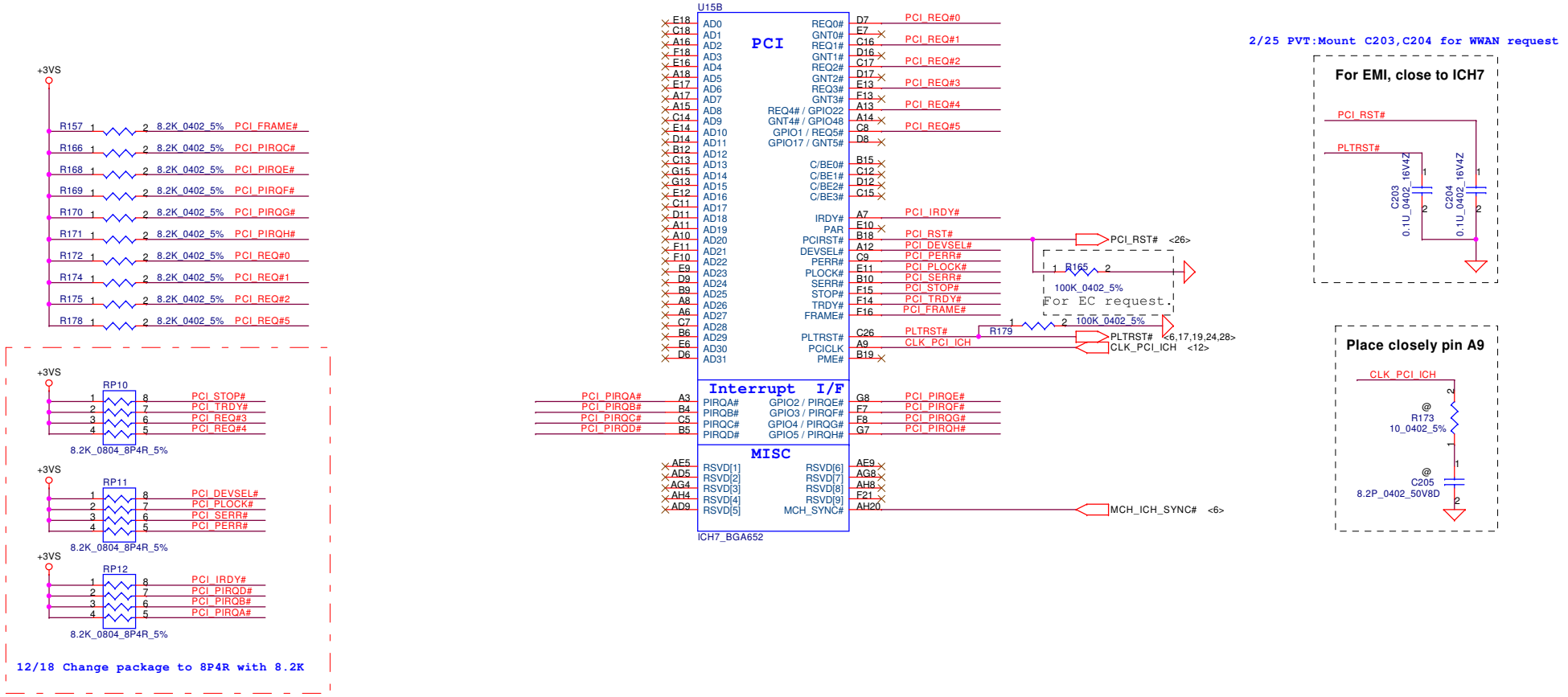

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Compal Electronics, Inc.

Title: ICH7M(1/4)HUB,PCI,HOST

Size | Document Number: KAVAA LA-5121P M/B | Rev: 1.0

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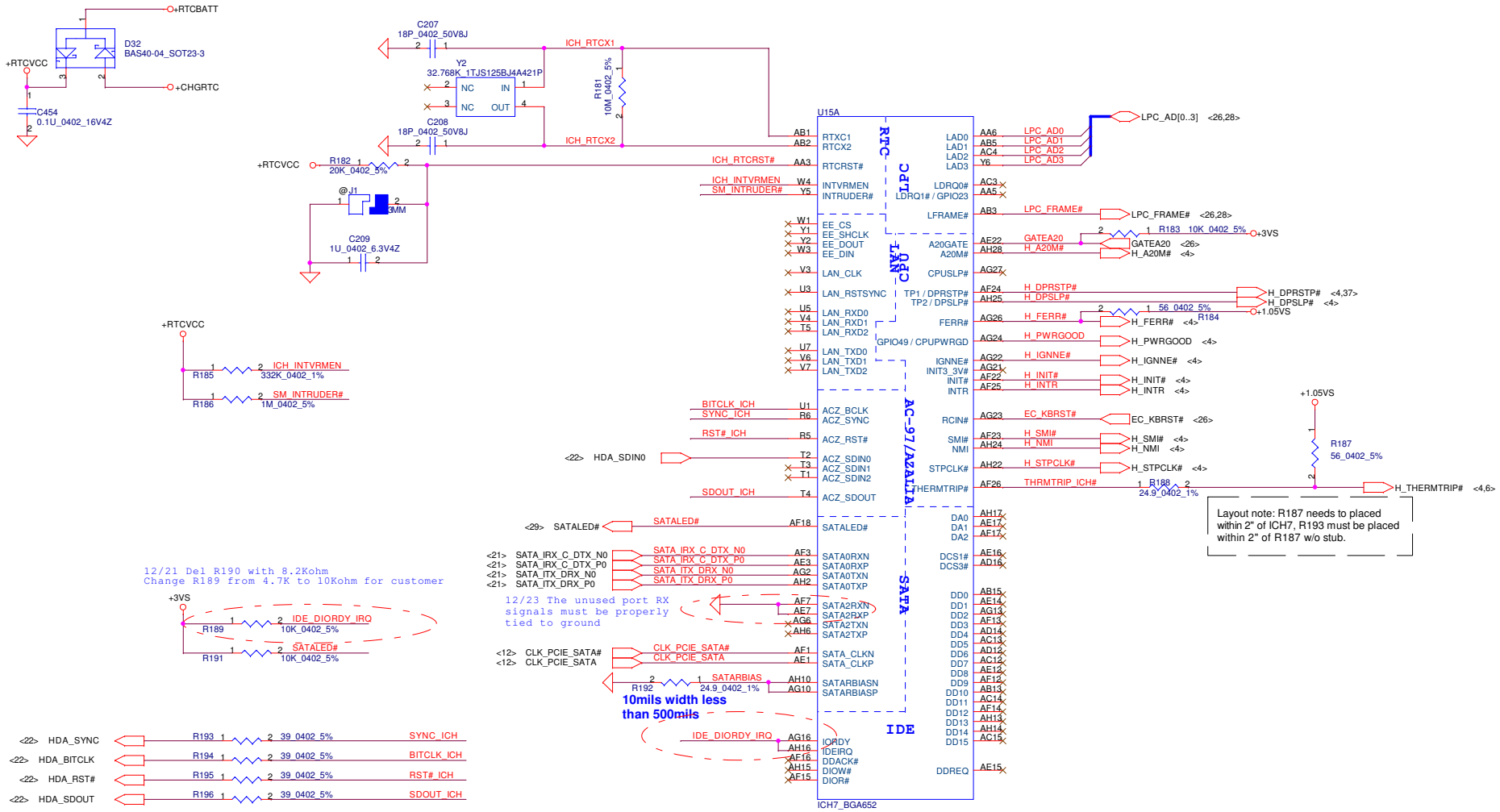

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: ICH7M(2/4)LAN,ATA,LPC,RTC

Size: Custom | Document Number: KAVAA LA-5121P M/B | Rev: 1.0

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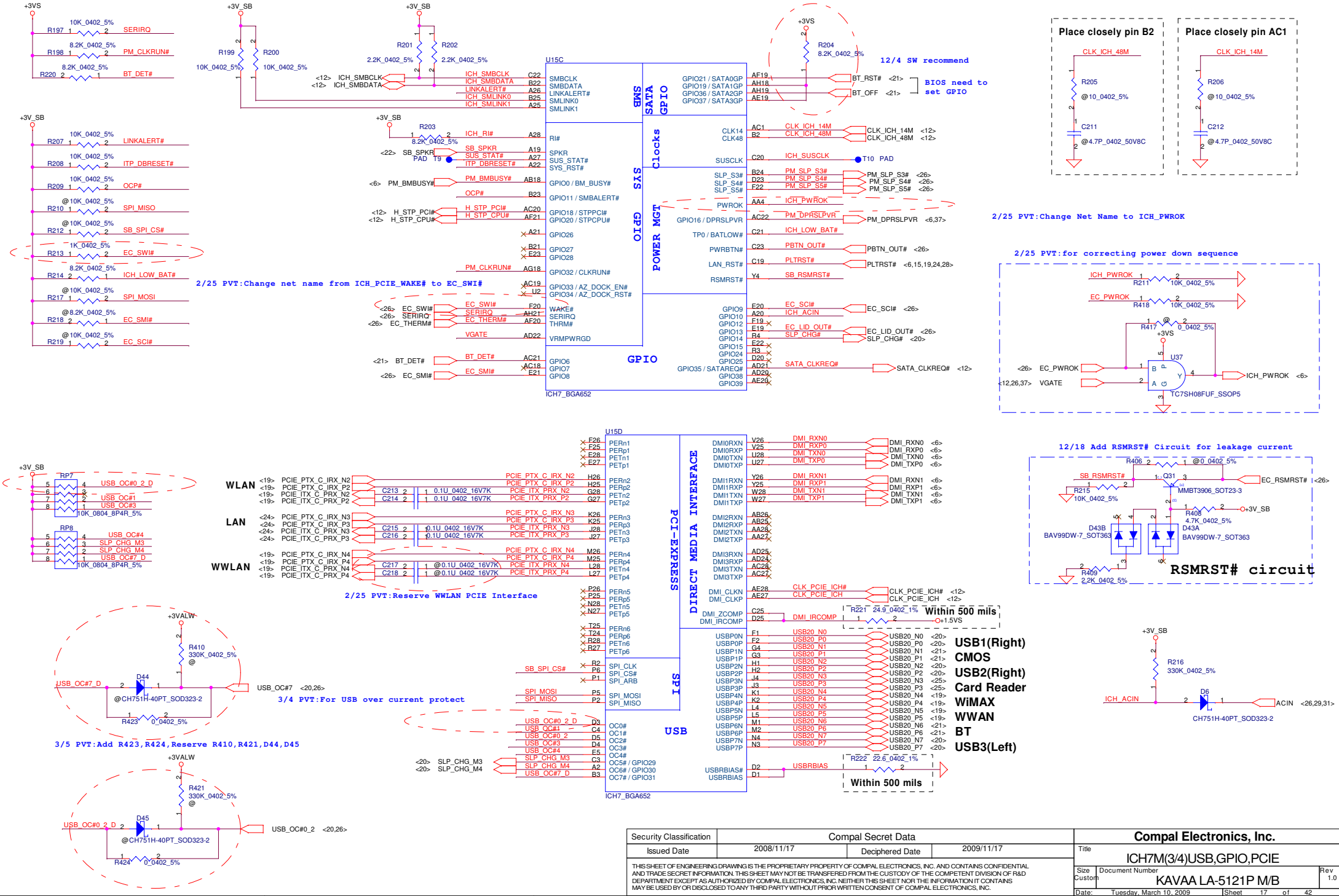

Security Classification	Compal Secret Data		
Issued Date	2008/11/17	Deciphered Date	2009/11/17

Compal Electronics, Inc.

Title: ICH7M(3/4)USB,GPIO,PCIE

Size	Document Number	Rev
Custom	KAVAA LA-5121P M/B	1.0

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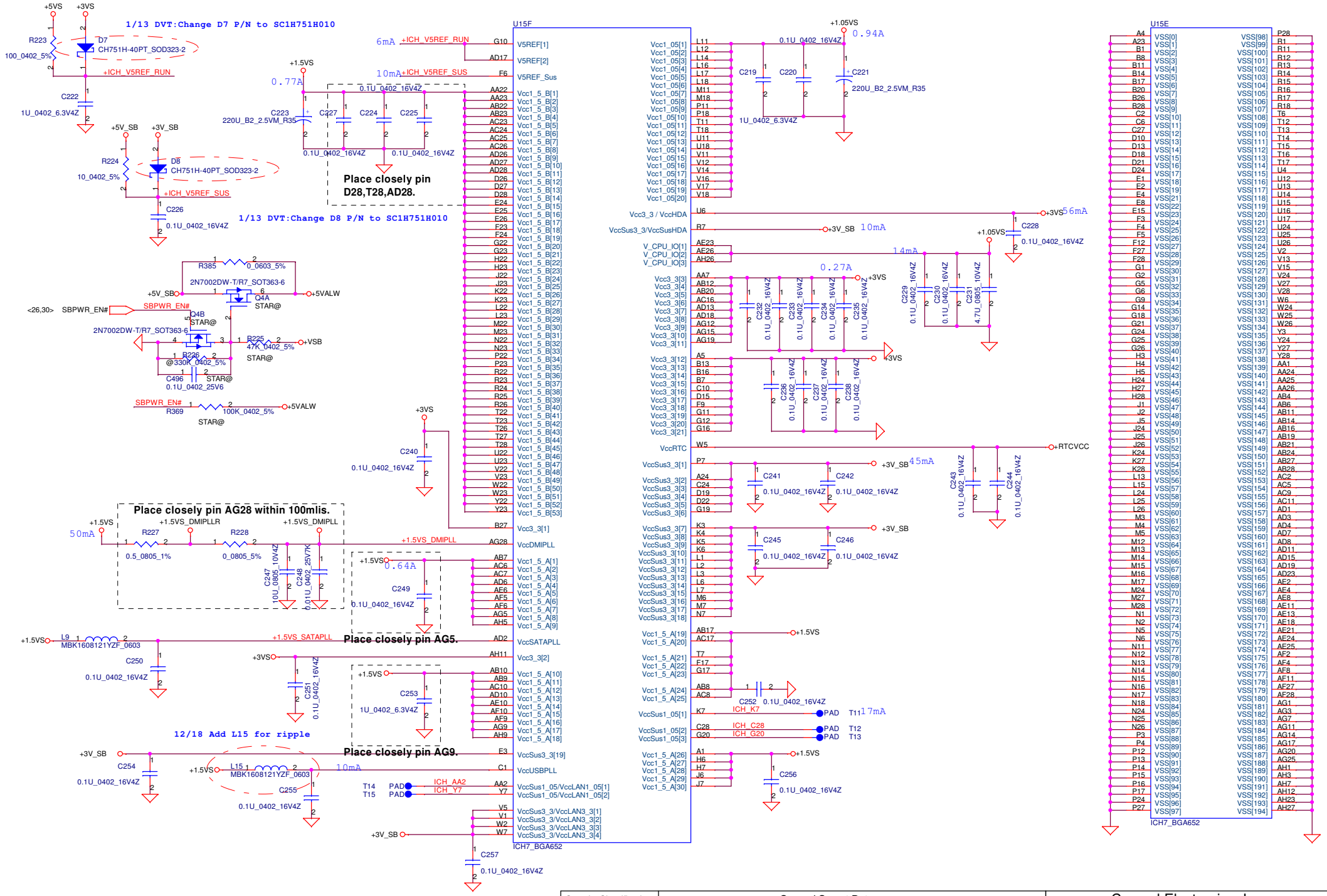

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: ICH7M(4/4)POWER/GND

Size: Custom | Document Number: KAVAA LA-5121P M/B | Rev: 1.0

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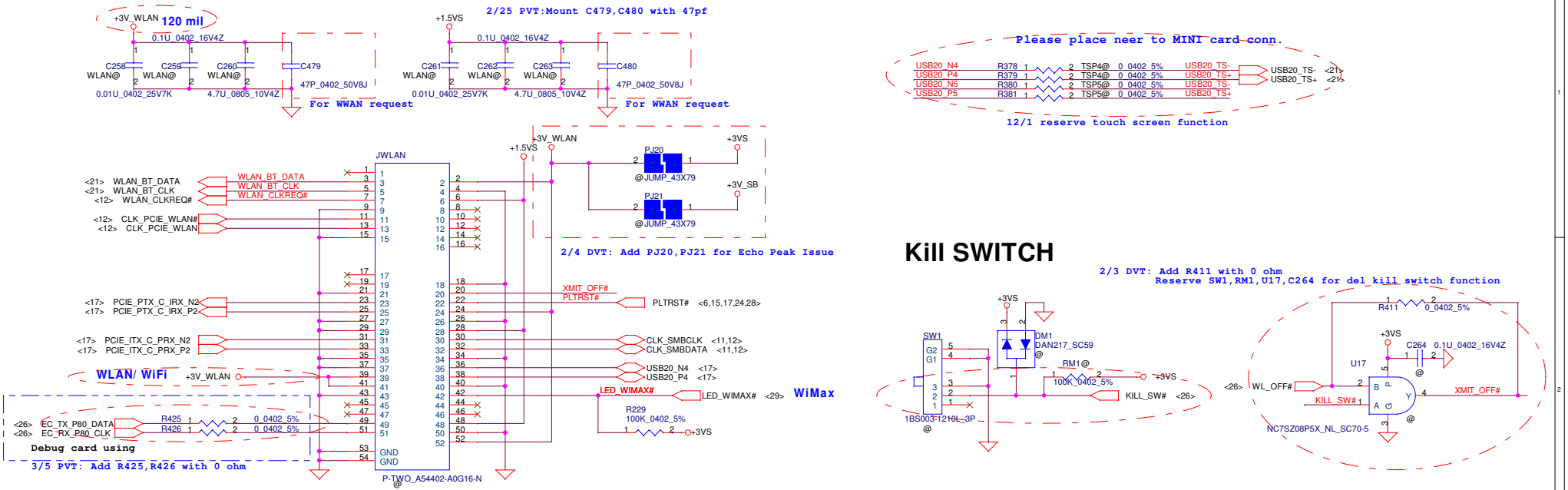
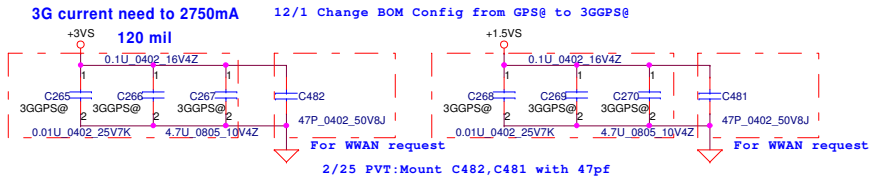
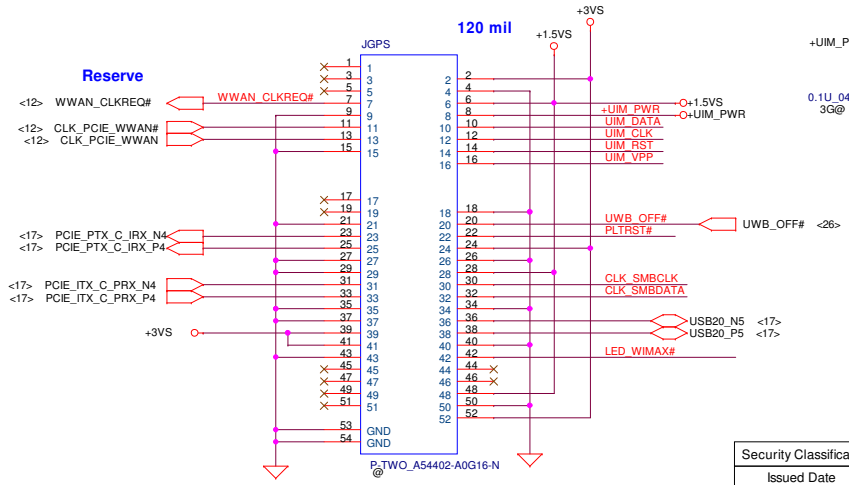
Mini-Express Card for WLAN/WiMax

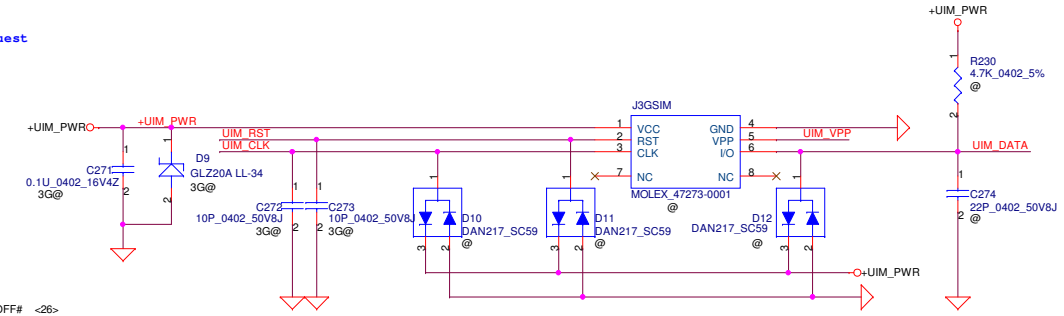


Kill SWITCH

Mini-Express Card for 3G/GPS







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Compal Electronics, Inc.	
Title	WLAN/WiMAX Express Slot
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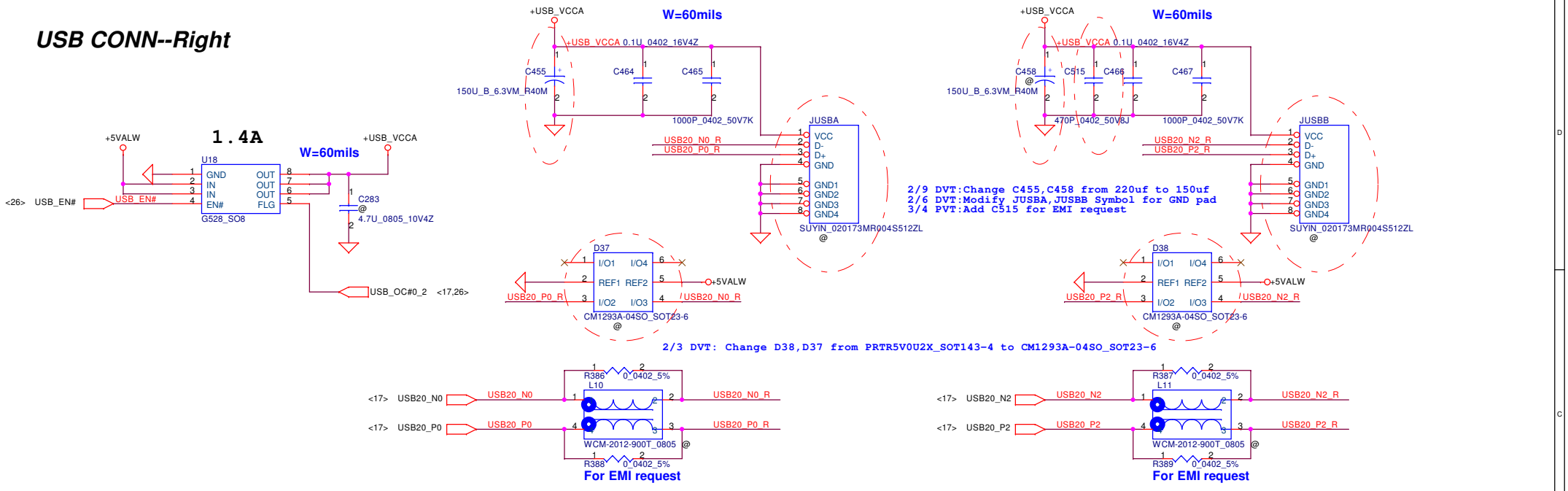
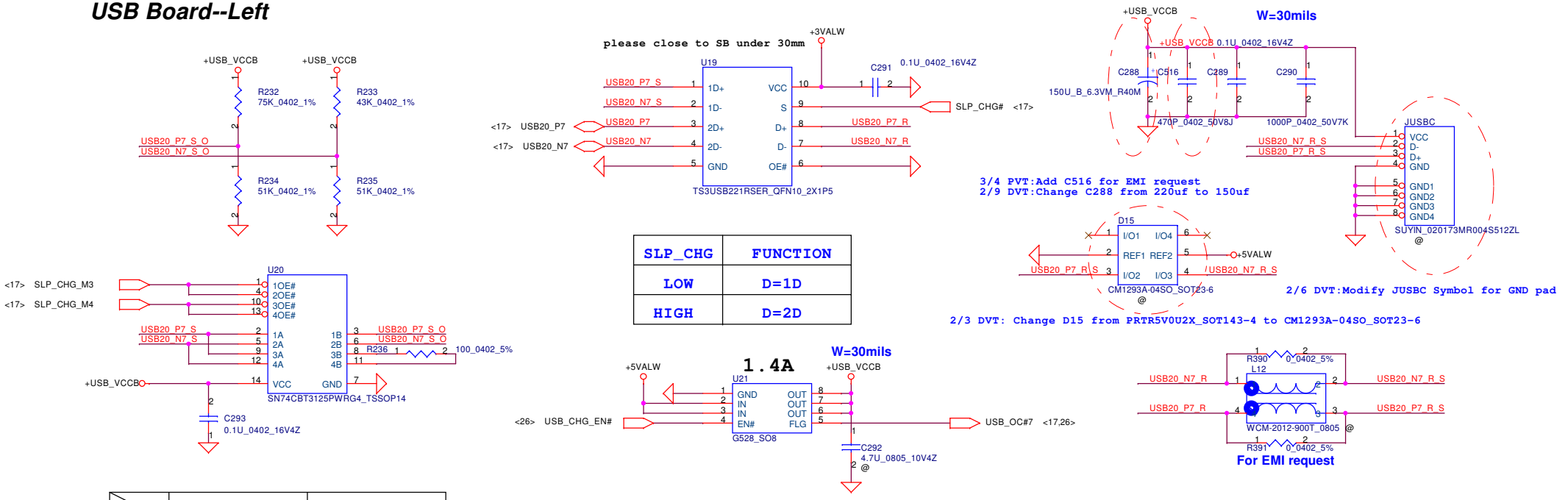
USB CONN--Right



USB Board--Left



SLP_CHG	FUNCTION
LOW	D=1D
HIGH	D=2D

	SLP_CHG_M3	SLP_CHG_M4
Mode 3	HIGH	LOW
Mode 4	LOW	HIGH

Security Classification	Compal Secret Data		
Issued Date	2008/11/17	Deciphered Date	2009/11/17

Compal Electronics, Inc.

Title: USB Conn

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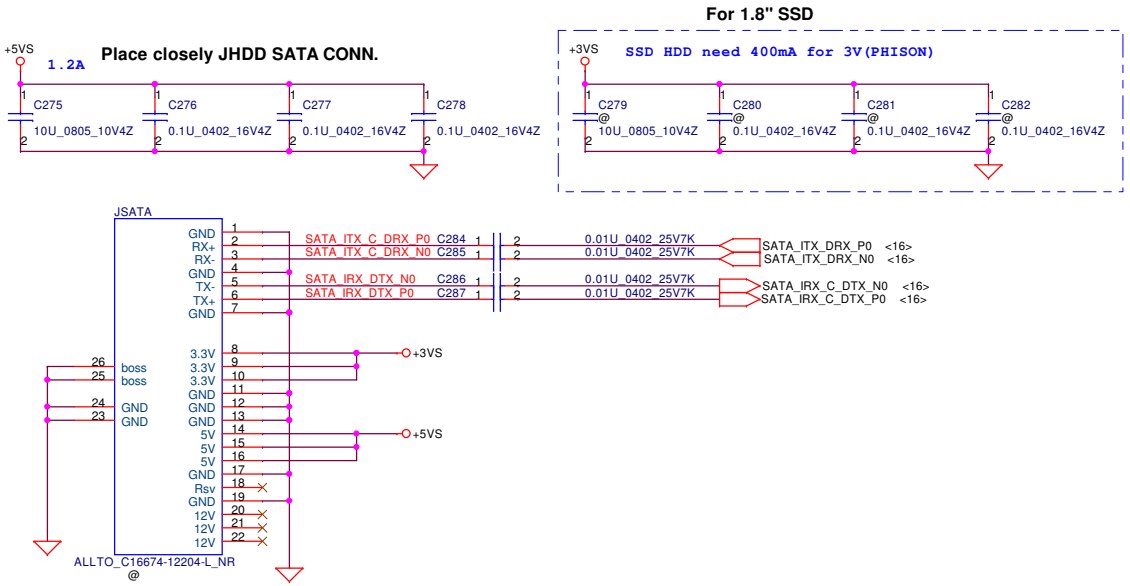
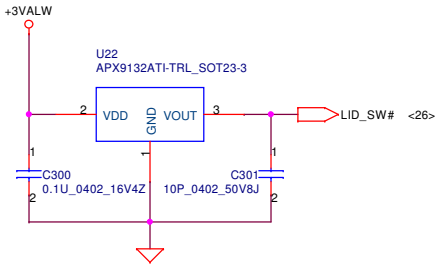
SATA Conn.

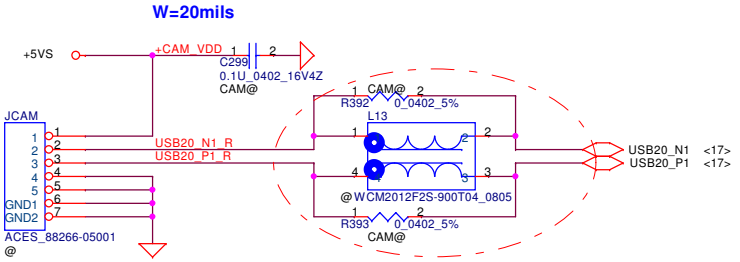


Lid SW

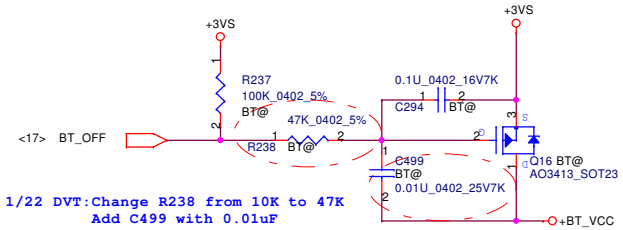


Camera Conn.

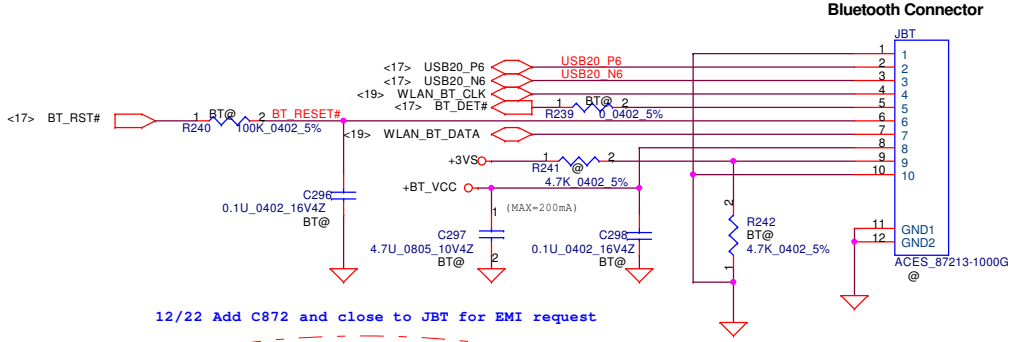
Int. Camera



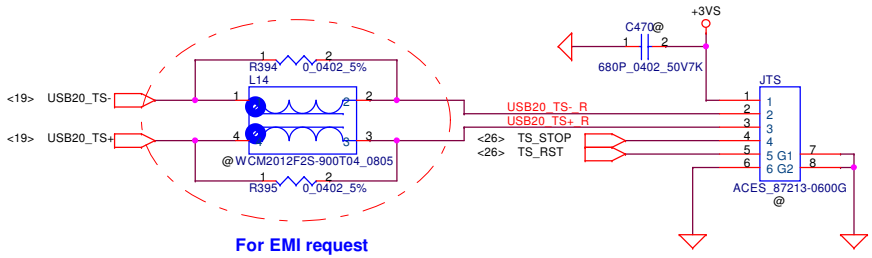
BlueTooth Interface



Bluetooth Connector



Touch Screen Conn.



Security Classification	Compal Secret Data		
Issued Date	2008/11/17	Deciphered Date	2009/11/17

Compal Electronics, Inc.

Title: SATA /BT/CMOS/TS/ Lid SW

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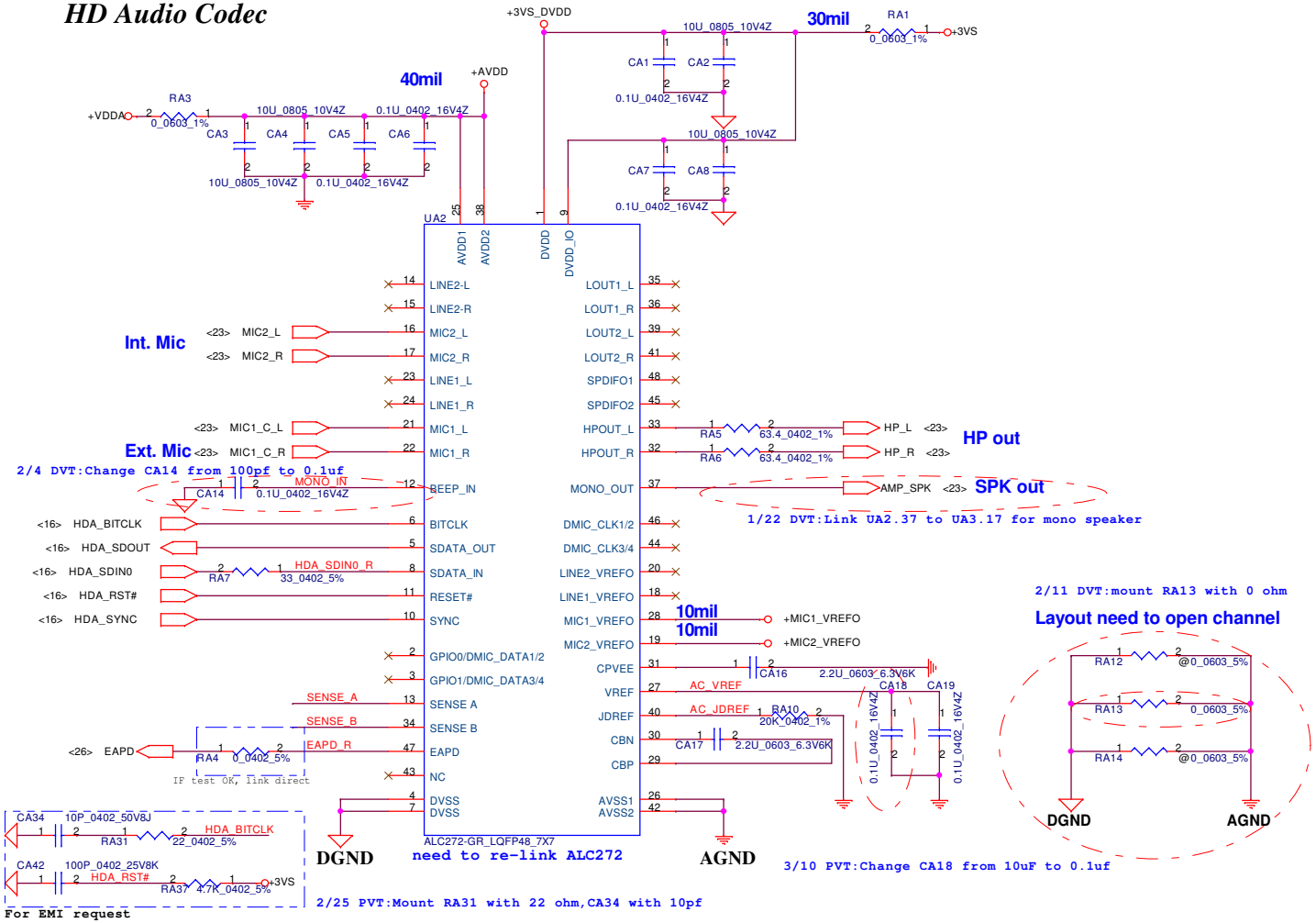
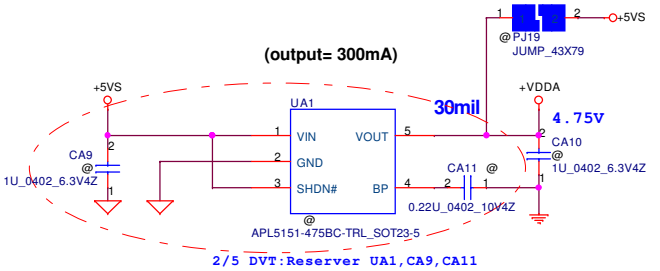
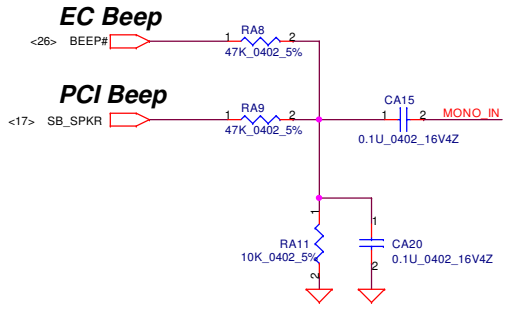
HD Audio Codec



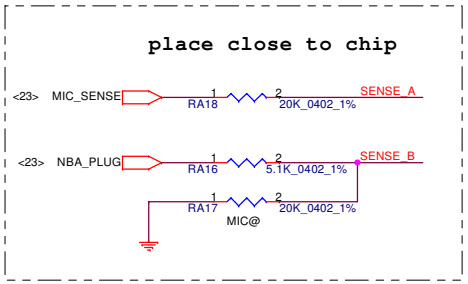
Audio regulator



Beep sound



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	PORT-D (PIN 35, 36)	SPK out
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	Headphone out



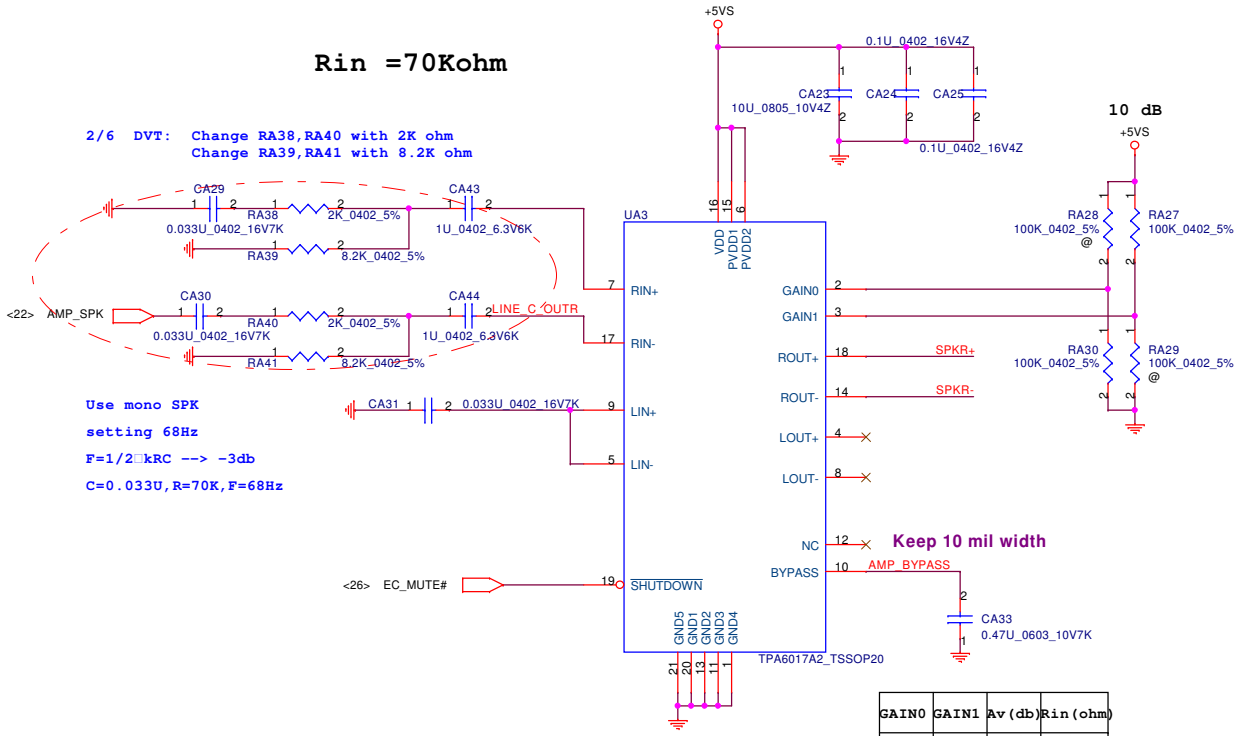
Security Classification	Compal Secret Data		
Issued Date	2008/11/17	Deciphered Date	2009/11/17

Compal Electronics, Inc.	
Title	ALC272-GR Codec
Size: Custom	Document Number: KAVAA LA-5121P M/B
Rev	1.0
Date: Tuesday, March 10, 2009	Sheet 22 of 42

TPA6017 Medium Range Amplifier

Rin =70Kohm

2/6 DVT: Change RA38,RA40 with 2K ohm
Change RA39,RA41 with 8.2K ohm

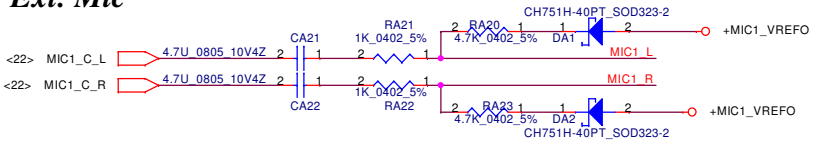


Use mono SPK
setting 68Hz
F=1/2□kRC --> -3db
C=0.033U,R=70K,F=68Hz

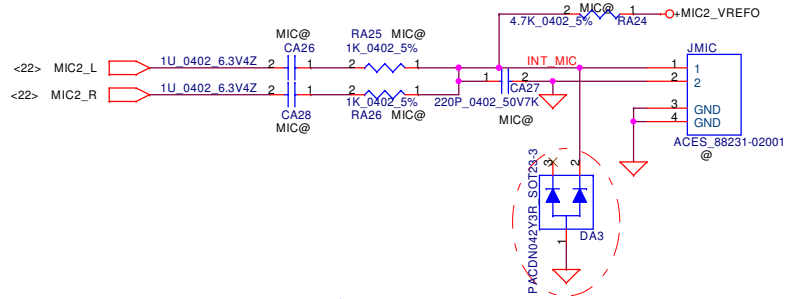
Keep 10 mil width

GAIN0	GAIN1	Av(db)	Rin(ohm)
0	0	6	90K
0	1	10	70K
1	0	15.6	45K
1	1	21.6	25K

Ext. Mic



Int. Mic

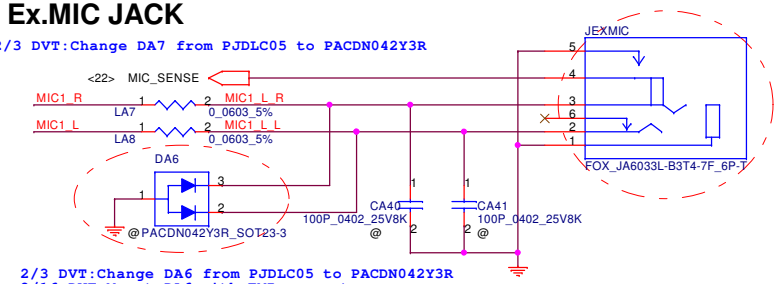


2/3 DVT:Change DA3 from PJDLC05 to PACDN042Y3R
2/16 DVT:Mount DA3 with EMI request

1/13 DVT:Change net name from JLINE to JEXMIC

Ex.MIC JACK

2/3 DVT:Change DA7 from PJDLC05 to PACDN042Y3R

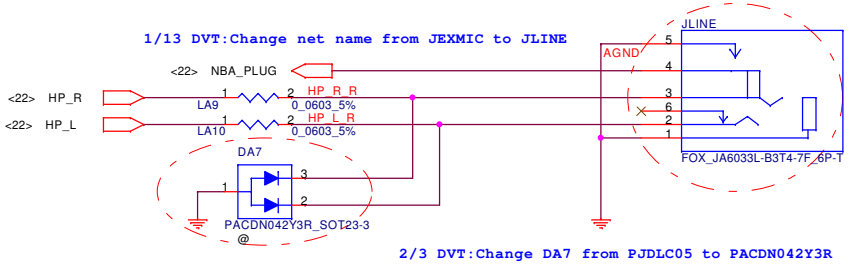


2/3 DVT:Change DA6 from PJDLC05 to PACDN042Y3R
2/16 DVT:Mount DA6 with EMI request
3/4 PVT:Reserve DA6 with PACDN042Y3R

2/25 PVT:Change JEXMIC,JLINE PCB footprint

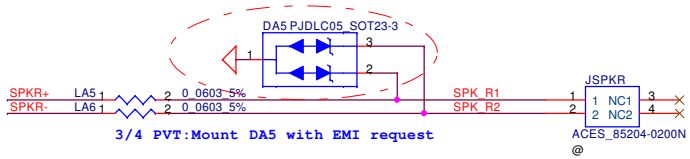
Head Phone JACK

1/13 DVT:Change net name from JEXMIC to JLINE



2/3 DVT:Change DA7 from PJDLC05 to PACDN042Y3R

Right Speaker Connector



3/4 PVT:Mount DA5 with EMI request

Security Classification	Compal Secret Data		
Issued Date	2008/11/17	Deciphered Date	2009/11/17

Compal Electronics, Inc.

Title: AMP/VR/Audio Jack/MIC

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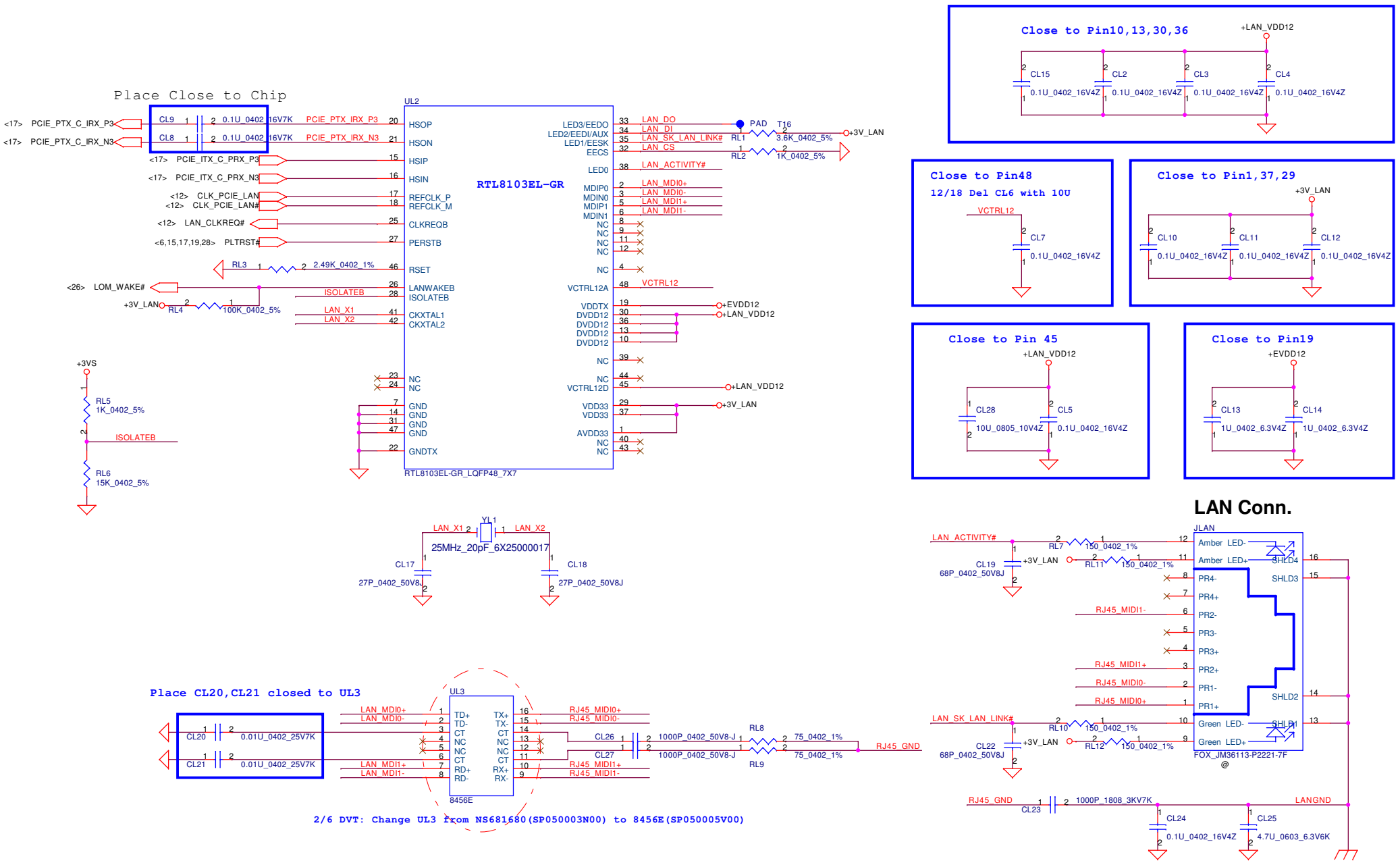

Security Classification	Compal Secret Data		
Issued Date	2008/11/17	Deciphered Date	2009/11/17

Compal Electronics, Inc.

Title: RTL8103EL 10/100 LAN

Size	Document Number	Rev
Custom	KAVAA LA-5121P M/B	1.0

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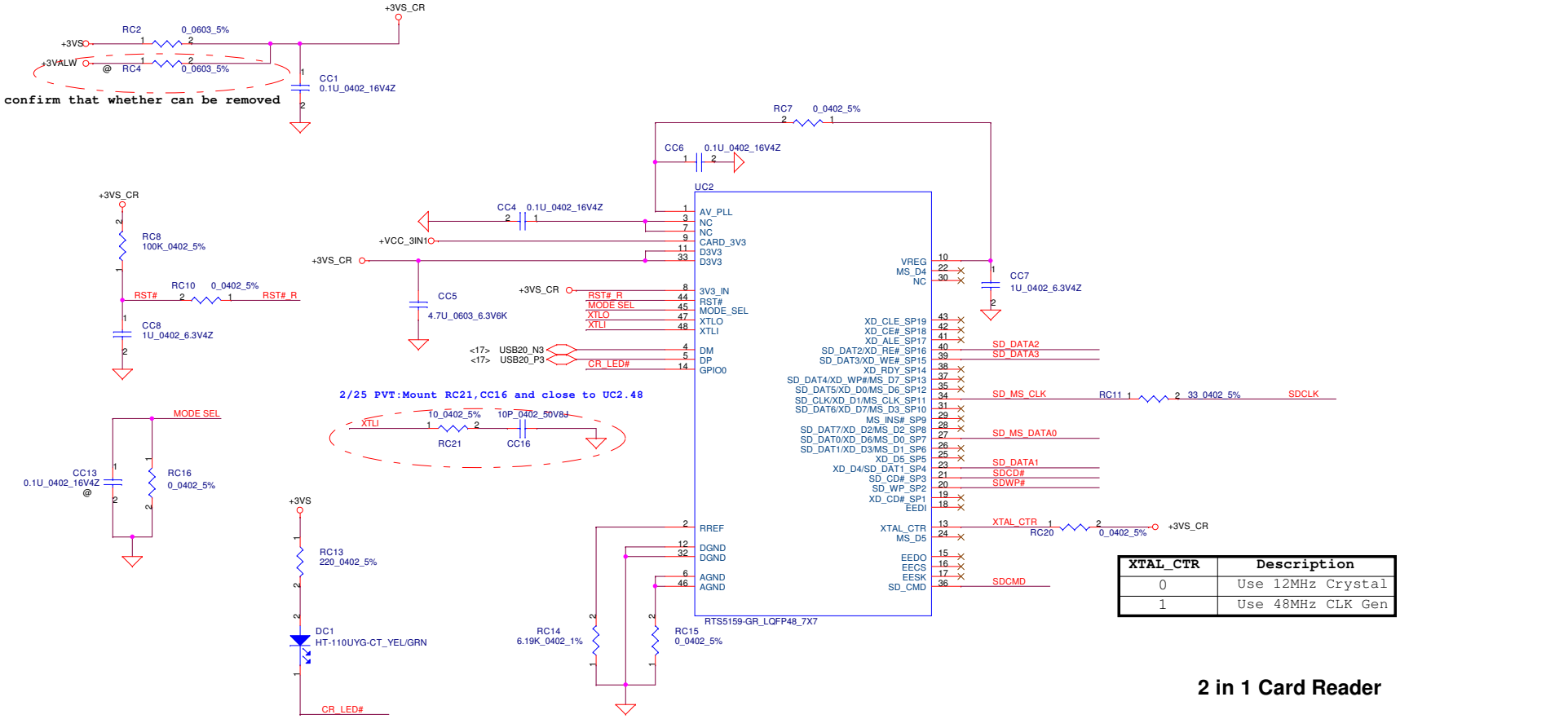
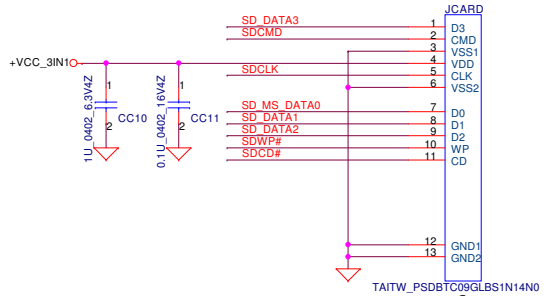
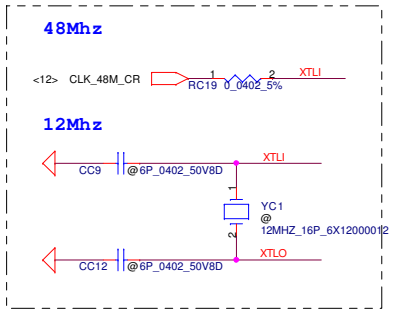


XTAL_CTR	Description
0	Use 12MHz Crystal
1	Use 48MHz CLK Gen

2 in 1 Card Reader





R	C	USB AUTO DE-LINK	MS FORMATTER	Description
0	NC	YES		Recommended
NC	47P	YES	YES	
NC	NC			Compatible with RTS5158E
NC	680P	YES		LED ON
10K	180P			LED ON
10K	680P		YES	

Security Classification	Compal Secret Data		
Issued Date	2008/11/17	Deciphered Date	2009/11/17

Compal Electronics, Inc.

Title: RTS5159 Card Reader

Size: Custom | Document Number: KAVAA LA-5121P M/B | Rev: 1.0

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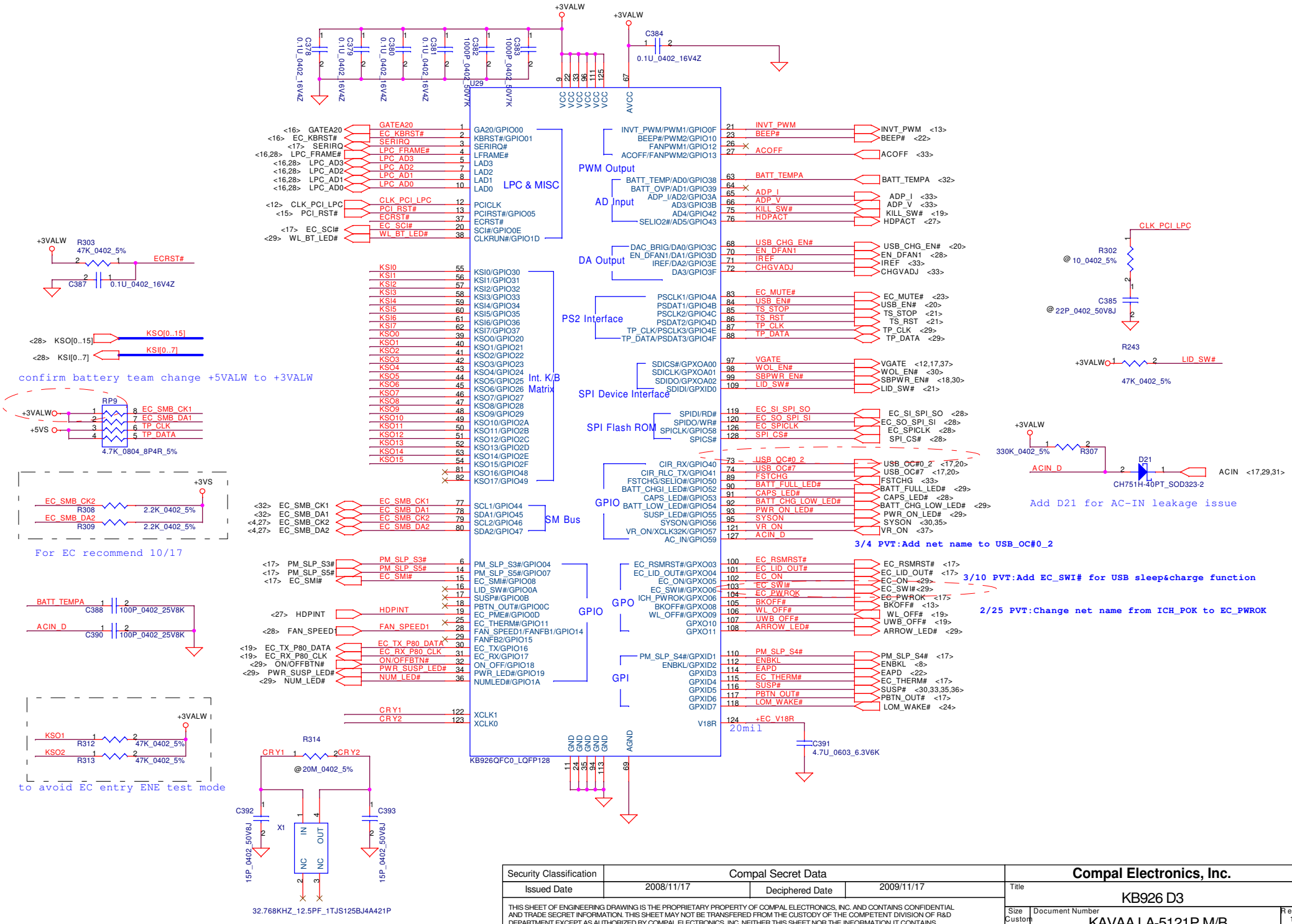

Security Classification	Compal Secret Data		
Issued Date	2008/11/17	Deciphered Date	2009/11/17

Compal Electronics, Inc.

Title: KB926 D3

Size	Document Number	Rev
Custom	KAVAA LA-5121P M/B	1.0

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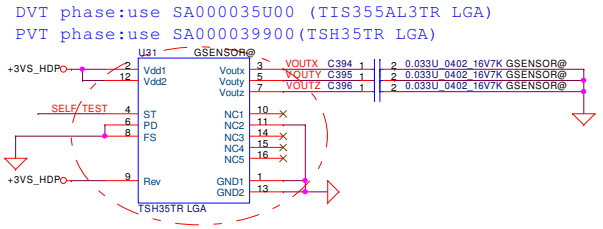
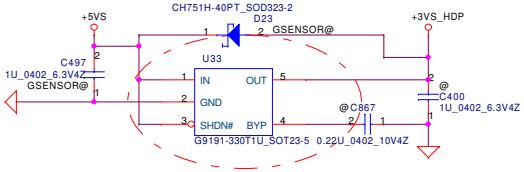
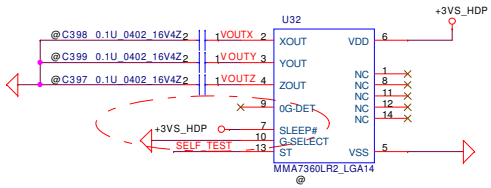
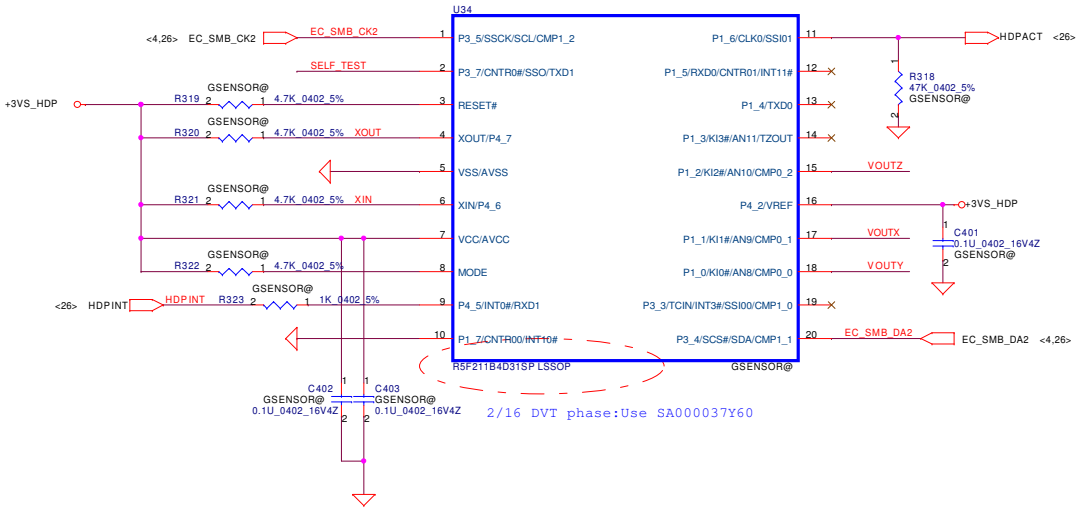
G-Sensor









Security Classification	Compal Secret Data		
Issued Date	2008/11/17	Deciphered Date	2009/11/17

Compal Electronics, Inc.

Title: **G-Sensor**

Size	Document Number	Rev
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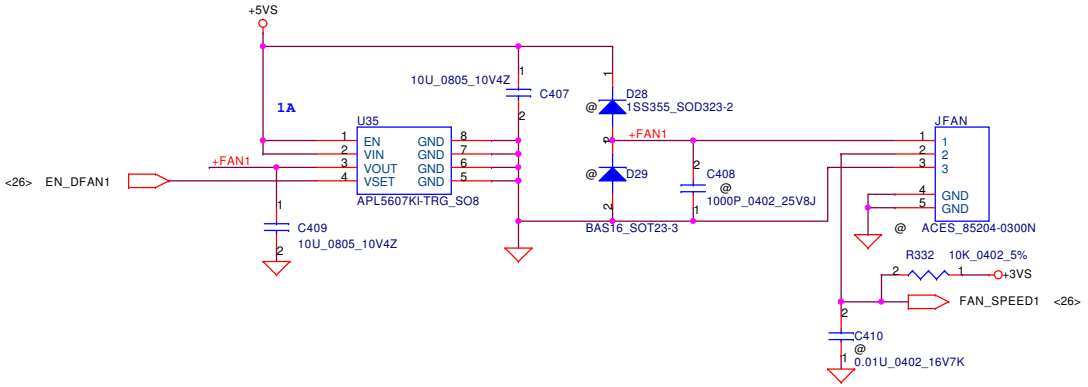
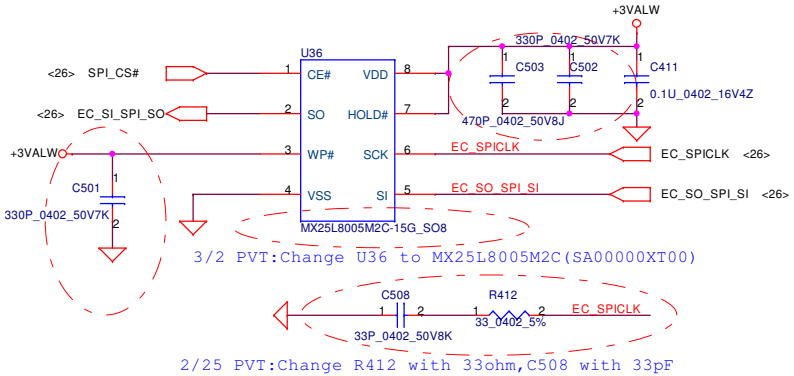
FAN Control Circuit



SPI Flash (8Mb*1)

2/3 DVT: Add C501,C502,C503,R412 for EMI request

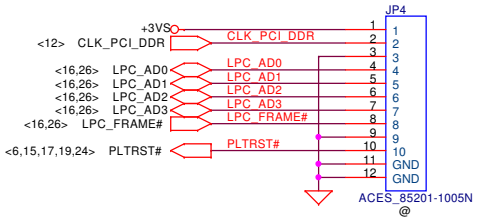


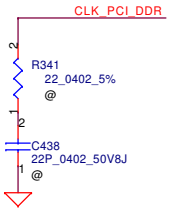
3/2 PVT:Change U36 to MX25L8005M2C(SA00000XT00)

2/25 PVT:Change R412 with 33ohm,C508 with 33pF

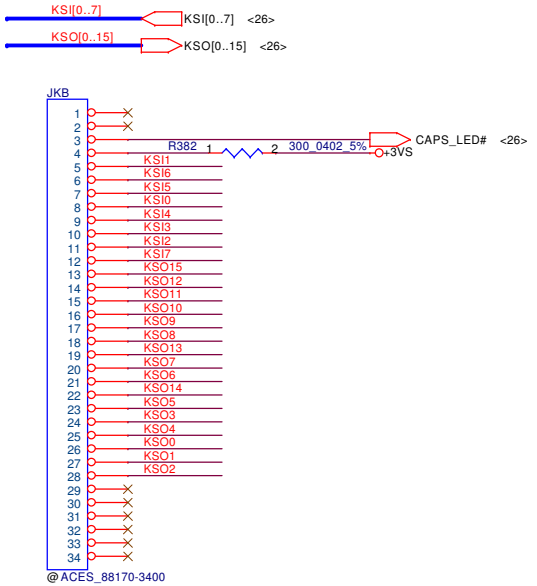
LPC Debug Port

Please place the connector neer to DDR door

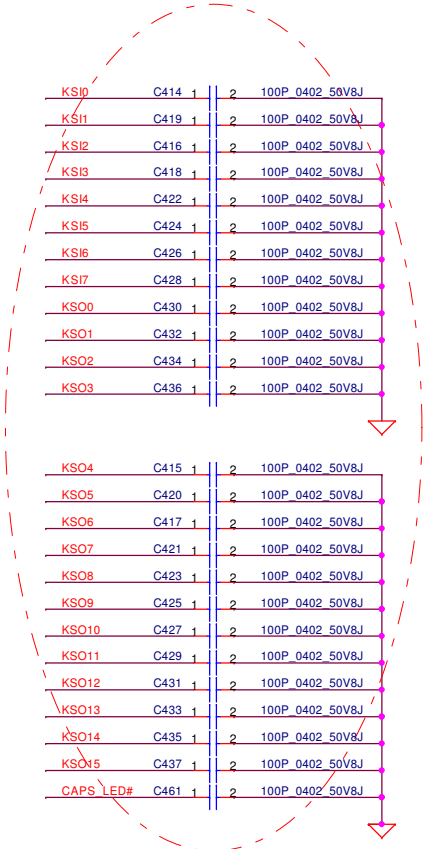




KEYBOARD CONN.



12/18 Follow KB Matrix the same to KSKAA



3/4 PVT:Mount C414~C437,C461 for EMI request

Security Classification	Compal Secret Data		
Issued Date	2008/11/17	Deciphered Date	2009/11/17

Title	SPI ROM//KB//FAN/Debug Poart		
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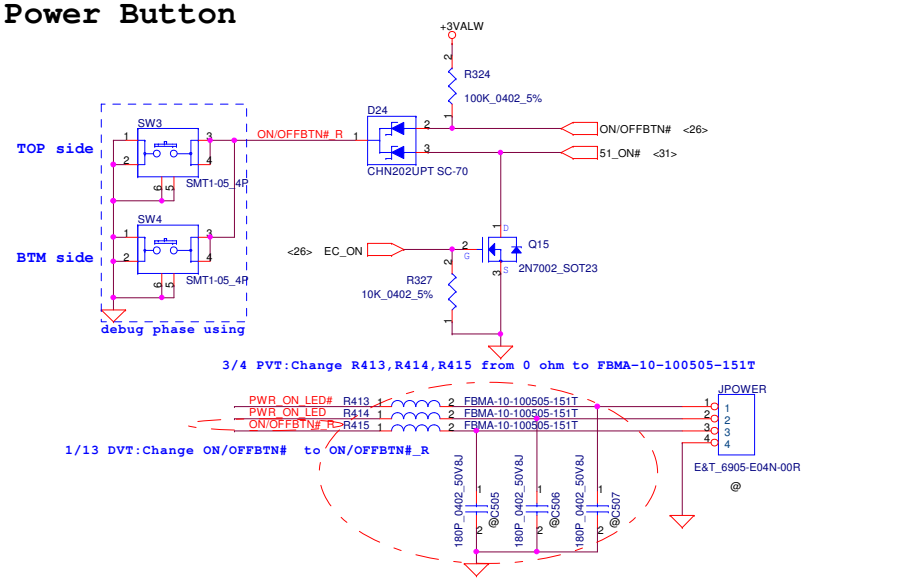
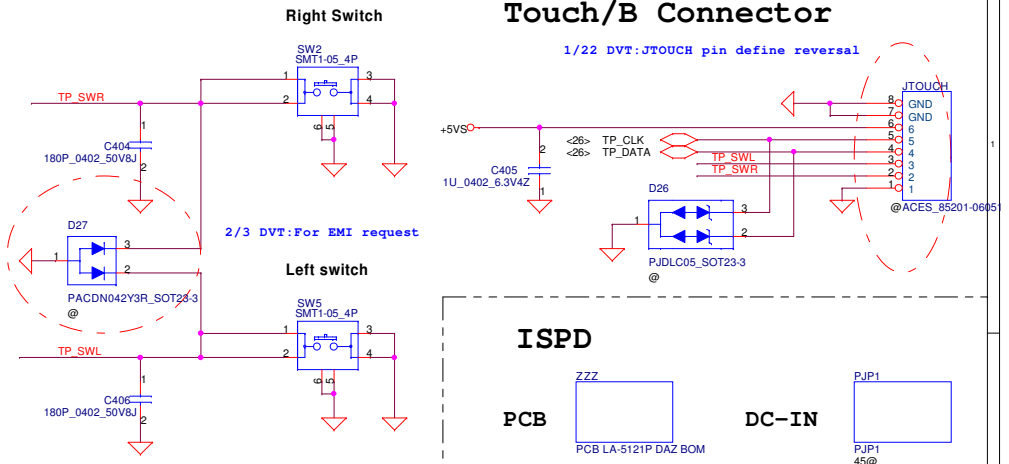
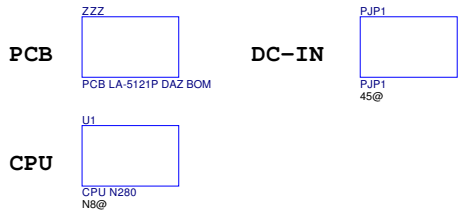
Power Button



Touch/B Connector

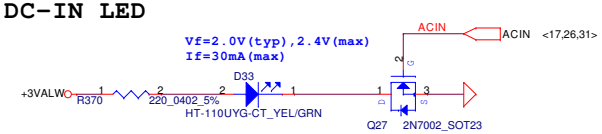


ISPD

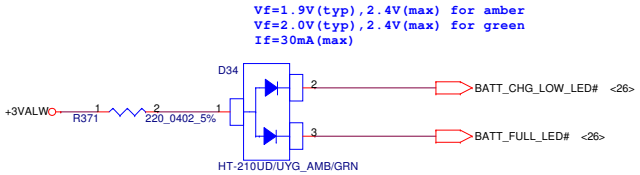


LED Conn

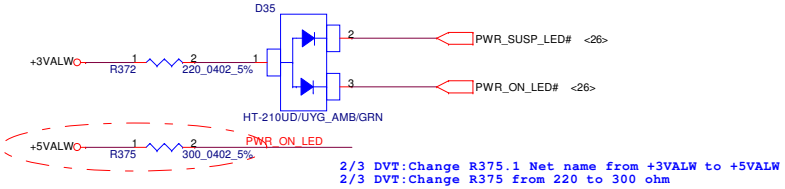
DC-IN LED



BATT CHARGE/FULL LED



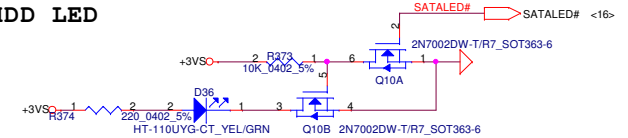
POWER/SUSPEND LED



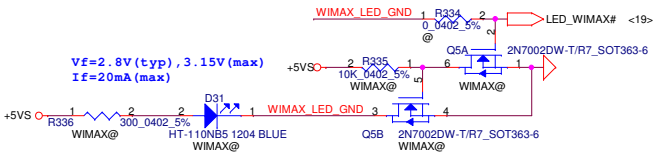
ARROW MODE LED

NUMERIC MODE LED

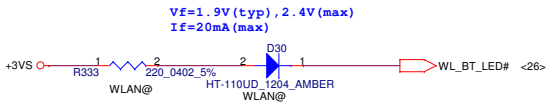
HDD LED



WiMAX&3G LED



WL&BT LED



Security Classification	Compal Secret Data		
Issued Date	2008/11/17	Deciphered Date	2009/11/17

Compal Electronics, Inc.

Title: ON/OFF /TP Conn/LEDS

Size: Custom | Document Number: KAVAA LA-5121P M/B | Rev: 1.0

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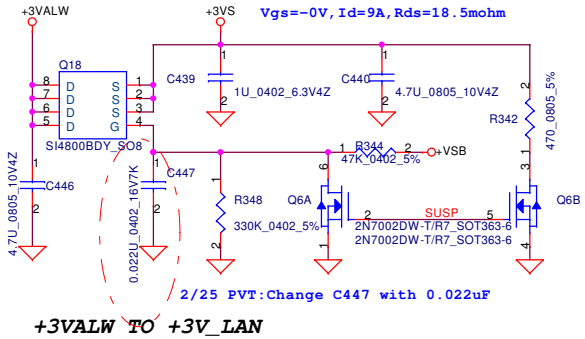
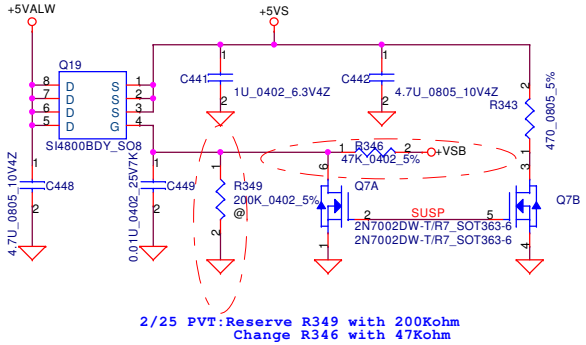
+3VALW TO +3VS



2/25 PVT:Change C447 with 0.022uF

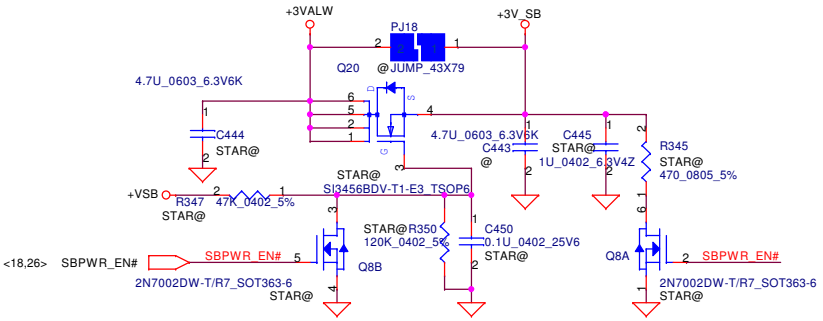
+5VALW TO +5VS



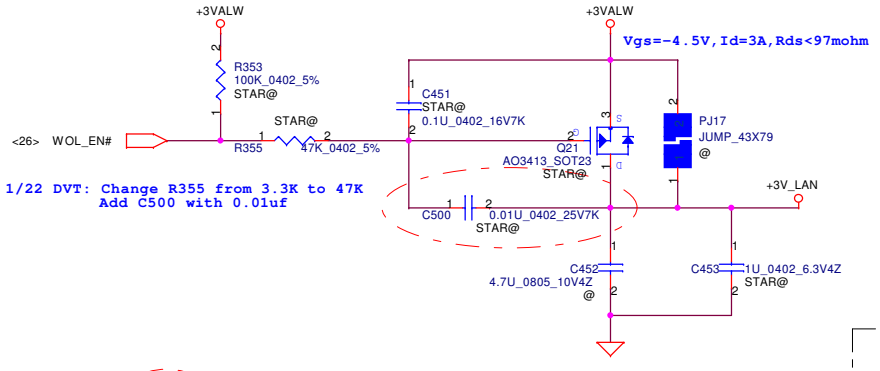
2/25 PVT:Reserve R349 with 200Kohm
Change R346 with 47Kohm

+3VALW TO +3V_SB

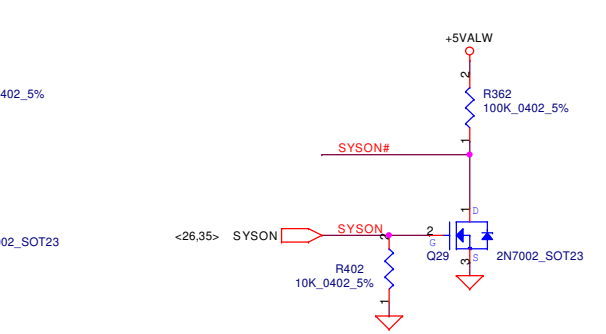
Vgs=10V,Id=6A,Rds=35mohm

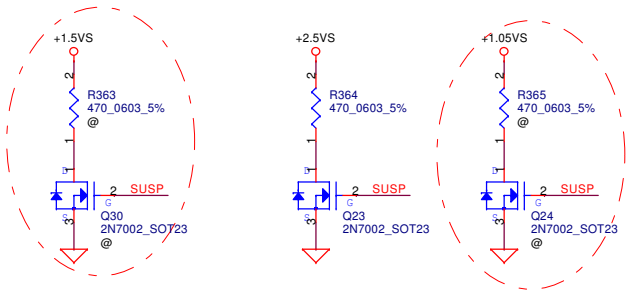


+3VALW TO +3V_LAN

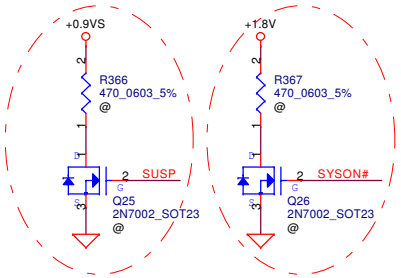


1/22 DVT: Change R355 from 3.3K to 47K
Add C500 with 0.01uf



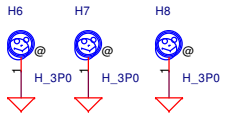


2/6 DVT: Reserve +1.5VS,+1.05VS,+0.9VS,+1.8VS discharge circuit

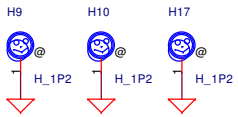


Screw Hole

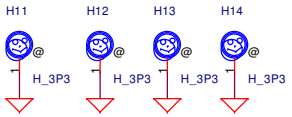
M/B



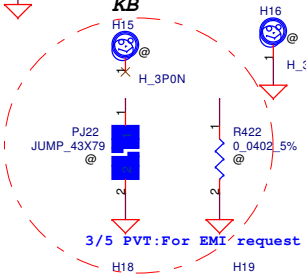
FAN



MINI Card
Full card



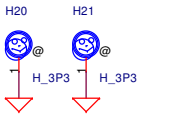
KB



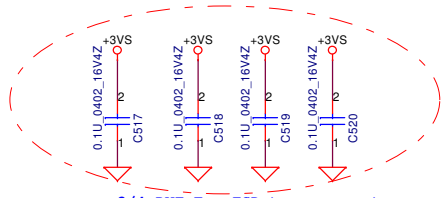
3/5 PVT:For EMI request

3/2 PVT:Change H18 from H_3P0N to H_2P6N
3/2 PVT:Change H19 from H_6P0X3P0N to H_6P0X2P6N

Half card

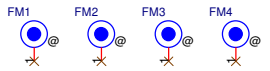


1/13 DVT:Add H20,H21 for half card



3/4 PVT:For ESD team request

FIDUCIAL_C40M80



Security Classification	Compal Secret Data		
Issued Date	2008/11/17	Deciphered Date	2009/11/17

Compal Electronics, Inc.

Title	DC INTERFACE	
Size: Custom	Document Number: KAVAA LA-5121P M/B	Rev: 1.0
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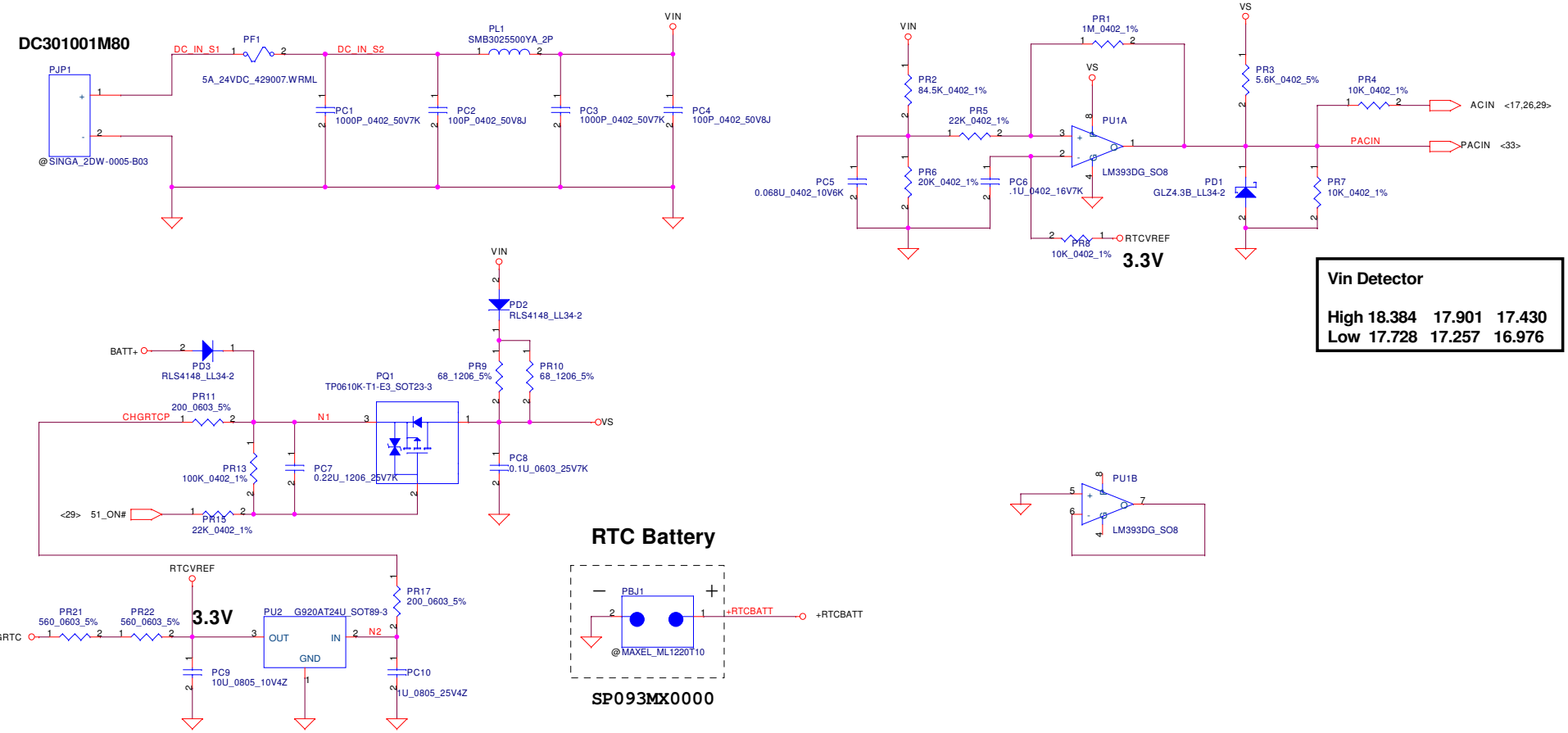

PJ1 @JUMP_43X118 — +3VALWP → +3VALW
(5A,200mils ,Via NO.= 10)
(OCP min=6.44A)

PJ2 @JUMP_43X118 — +1.8VP → +1.8V
(5A,200mils ,Via NO.= 10)
(OCP min=6.07A)

PJ3 @JUMP_43X118 — +5VALWP → +5VALW
(5A,200mils ,Via NO.= 10)
(OCP min=6.53A)

PJ4 @JUMP_43X118 — +1.05VSP → +1.05VS
(6A,240mils ,Via NO.=12)
(OCP min=7.55A)

PJ5 @ JUMP_43X39 — +VSBP → +VSB
(120mA,40mils ,Via NO.= 1)

PJ6 @JUMP_43X79 — +1.5VSP → +1.5VS
(3A,120mils ,Via NO.=6)

PJ7 @JUMP_43X79 — +0.9VSP → +0.9VS
(2A,80mils ,Via NO.= 4)

PJ8 @JUMP_43X39 — +2.5VSP → +2.5VS
(100mA,40mils ,Via NO.= 2)

Security Classification	Compal Secret Data		
Issued Date	2008/11/17	Deciphered Date	2009/11/17

Compal Electronics, Inc.

Title: DCIN&DECTOR

Size | Document Number: KAVAA LA-5121P M/B | Rev: 1.0

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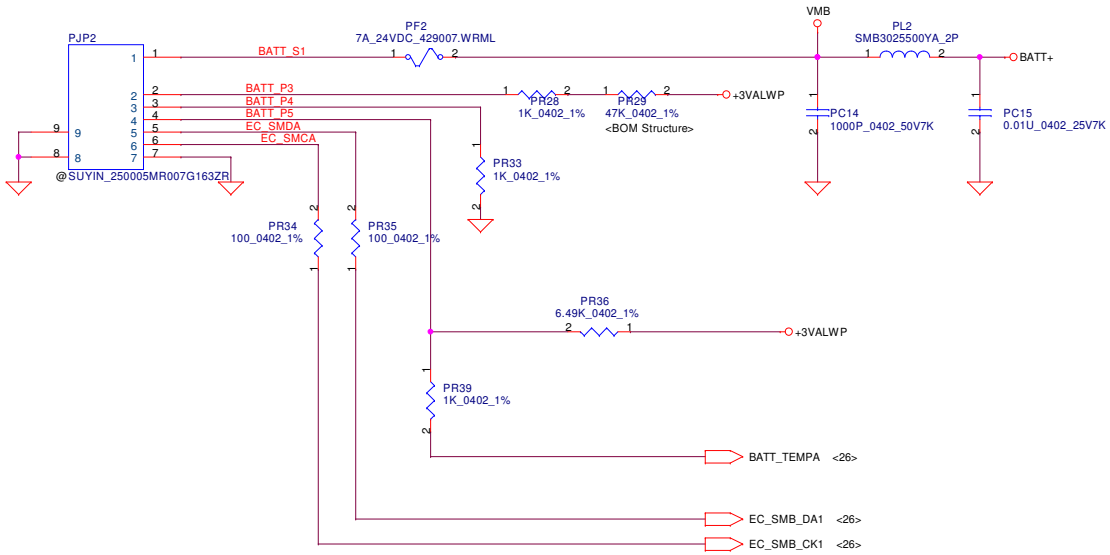
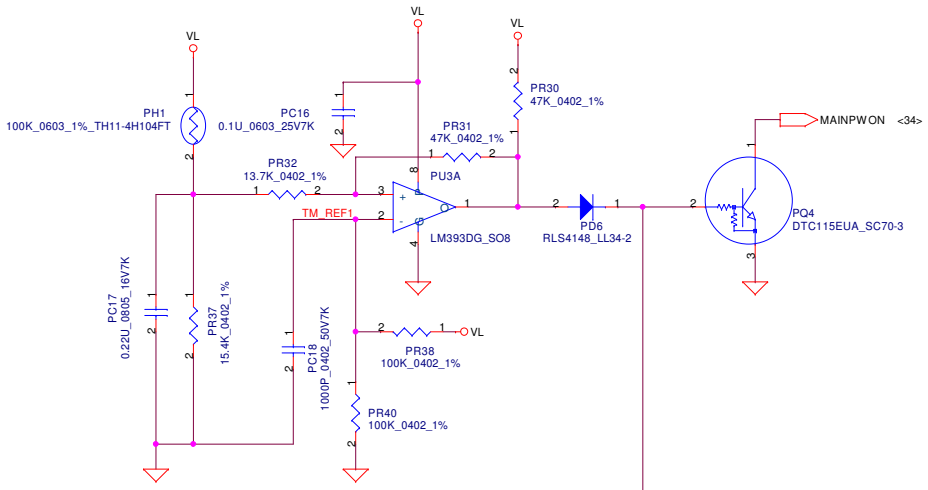
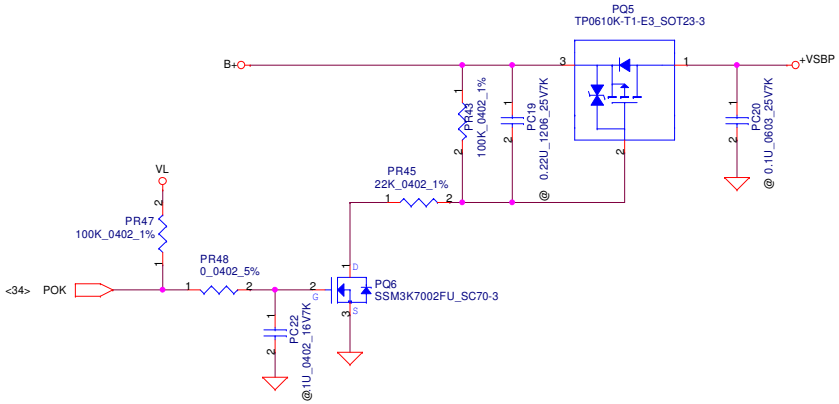
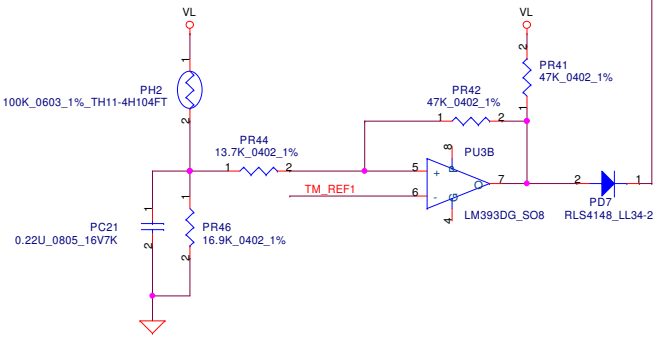
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C





PH2 near main Battery CONN :
BAT. thermal protection at 90 degree C
Recovery at 53 degree C





Security Classification	Compal Secret Data		
Issued Date	2008/11/17	Deciphered Date	2009/11/17

Compal Electronics, Inc.

Title: BATTERY CONN/OTP

Size	Document Number	Rev
	KAVAA LA-5121P M/B	1.0

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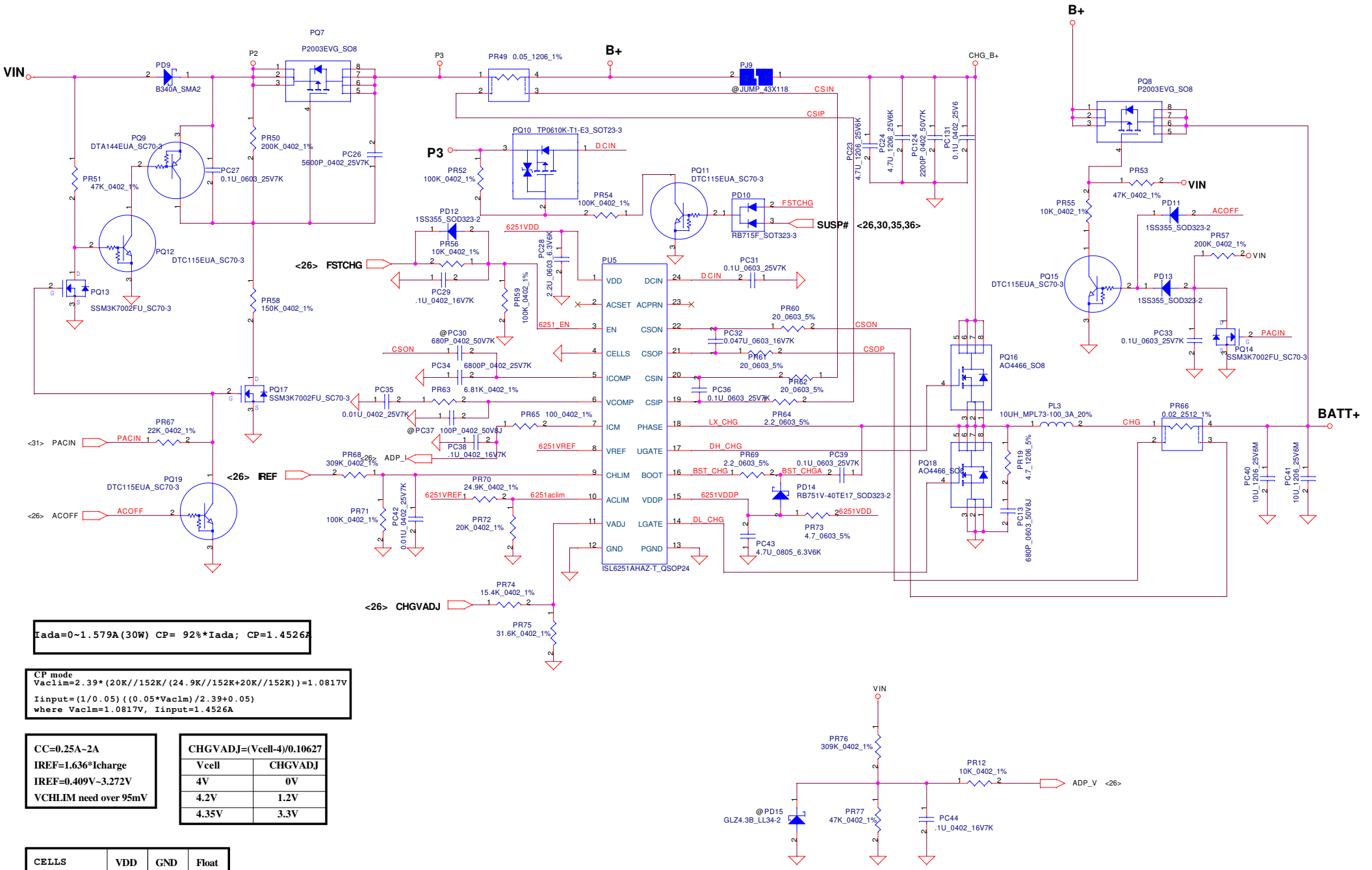


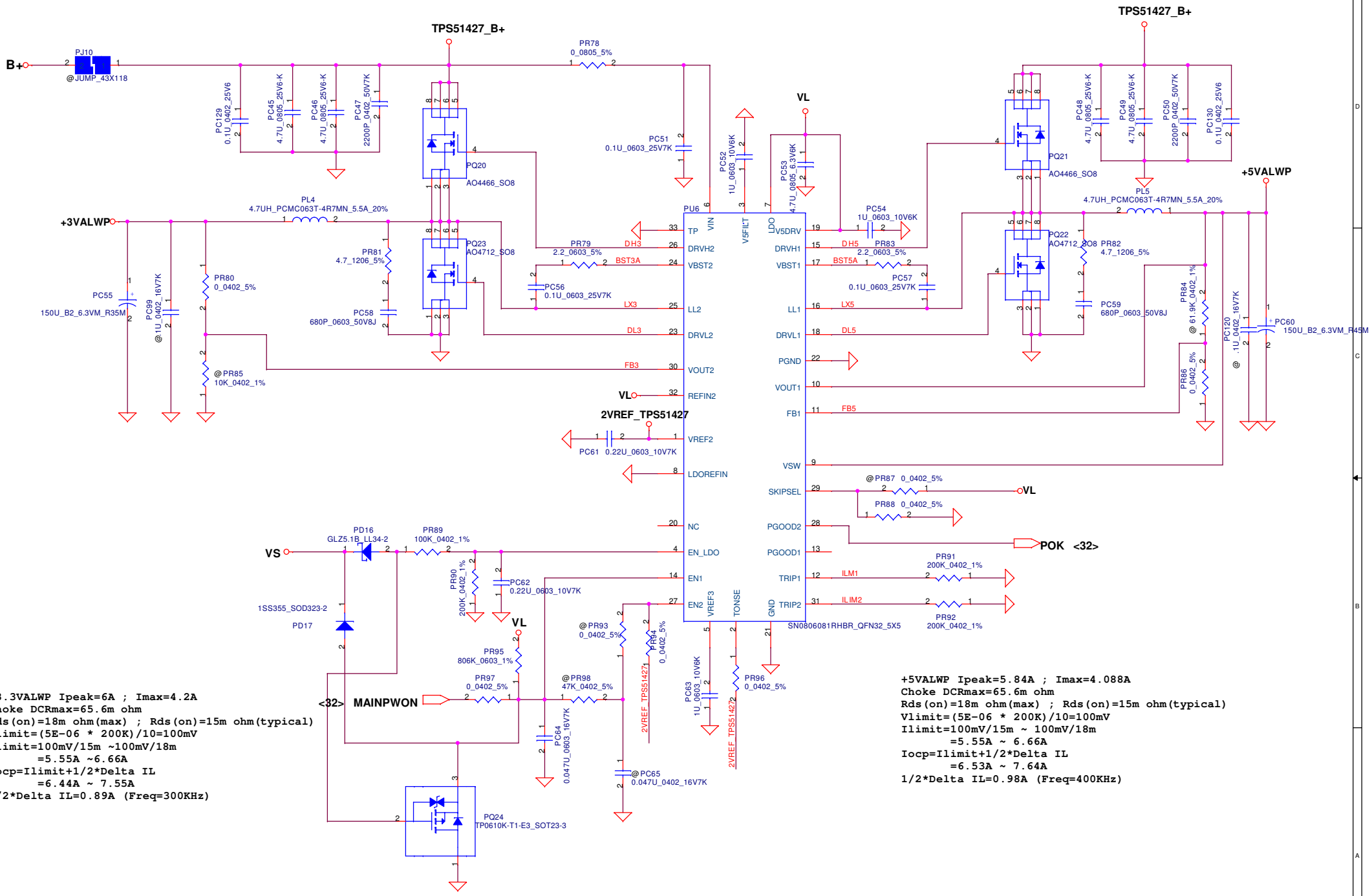
Security Classification	Compal Secret Data		
Issued Date	2008/11/17	Deciphered Date	2009/11/17

Compal Electronics, Inc.

Title: CHARGER

Size | Document Number: KAVAA LA-5121P M/B | Rev: 1.0

Date: Tuesday, March 10, 2009 | Sheet 33 of 42



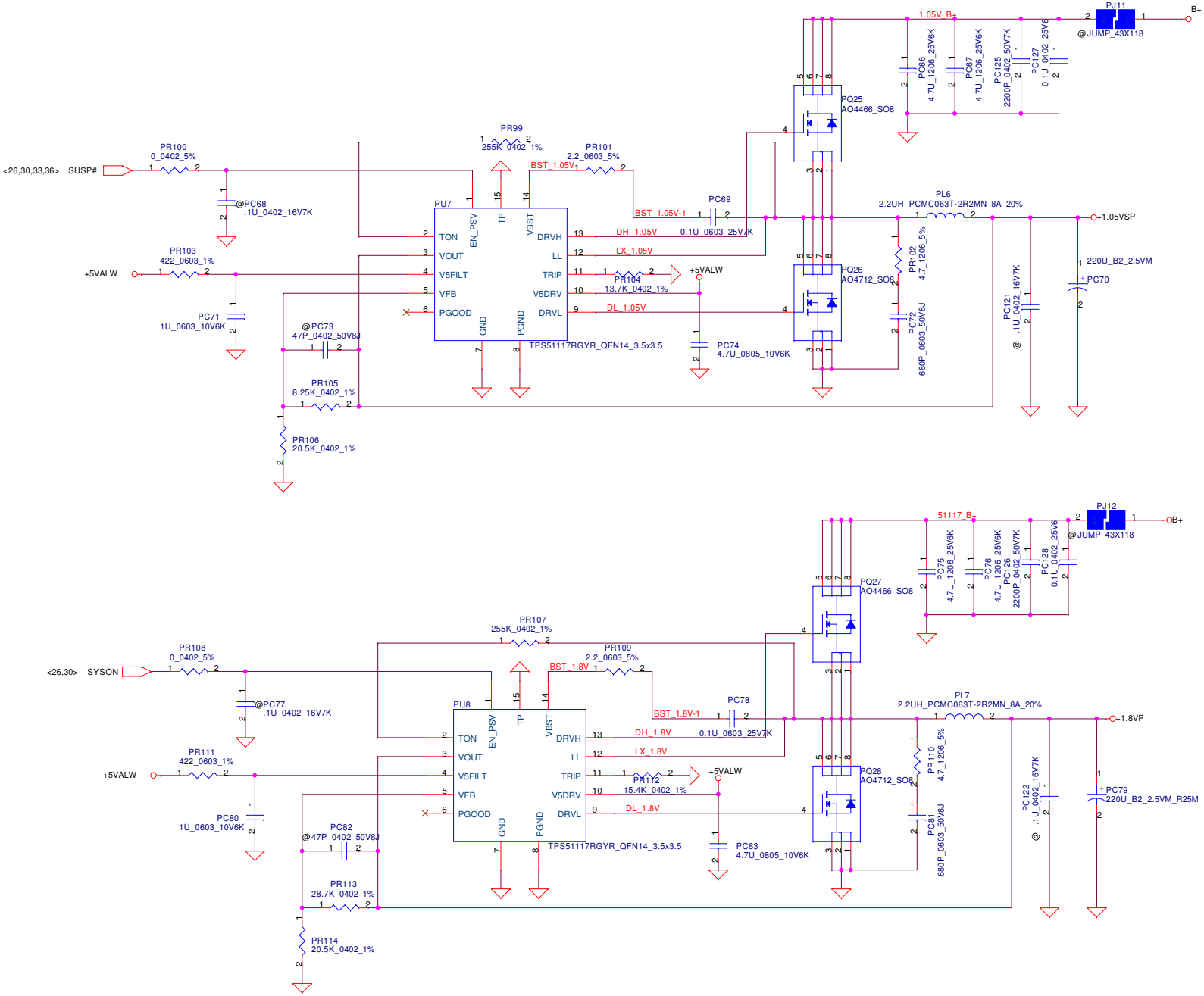
+3.3VALWP Ipeak=6A ; Imax=4.2A
Choke DCRmax=65.6m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 200K)/10=100mV
Ilimit=100mV/15m ~100mV/18m
=5.55A ~6.66A
Iocp=Ilimit+1/2*Delta IL
=6.44A ~ 7.55A
1/2*Delta IL=0.89A (Freq=300KHz)

+5VALWP Ipeak=5.84A ; Imax=4.088A
Choke DCRmax=65.6m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 200K)/10=100mV
Ilimit=100mV/15m ~ 100mV/18m
=5.55A ~ 6.66A
Iocp=Ilimit+1/2*Delta IL
=6.53A ~ 7.64A
1/2*Delta IL=0.98A (Freq=400KHz)

Security Classification	Compal Secret Data		
Issued Date	2008/11/17	Deciphered Date	2009/11/17

Compal Electronics, Inc.

Title	+5VALWP/+3VALWP	
Size	Document Number	Rev
	KAVAA LA-5121P M/B	1.0
Date: Tuesday, March 10, 2009	Sheet 34 of 42	



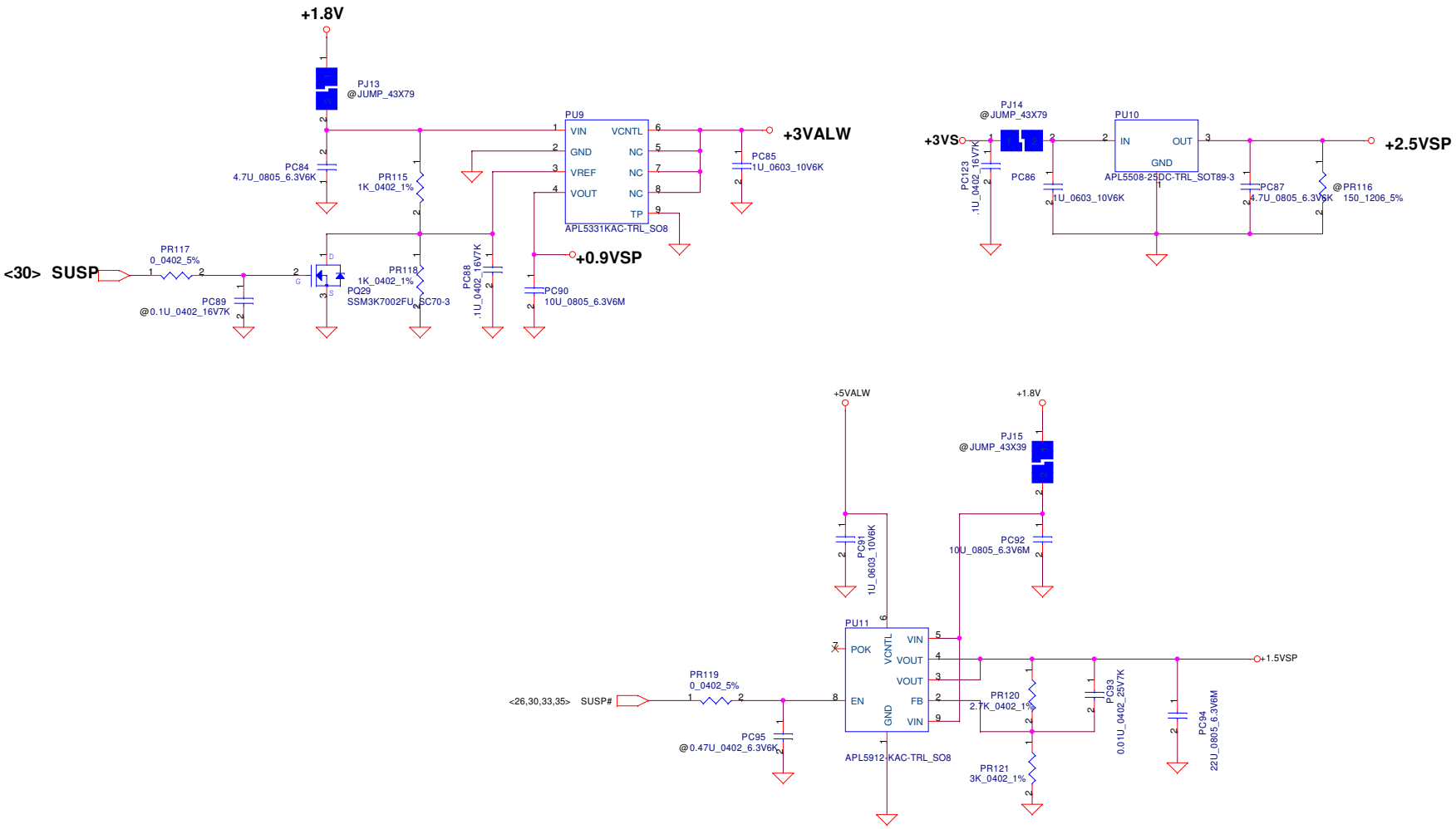
Security Classification	Compal Secret Data		
Issued Date	2008/11/17	Deciphered Date	2009/11/17

Compal Electronics, Inc.

Title: 1.05VSP/1.8VP

Size	Document Number	Rev
	KAVAA LA-5121P M/B	1.0

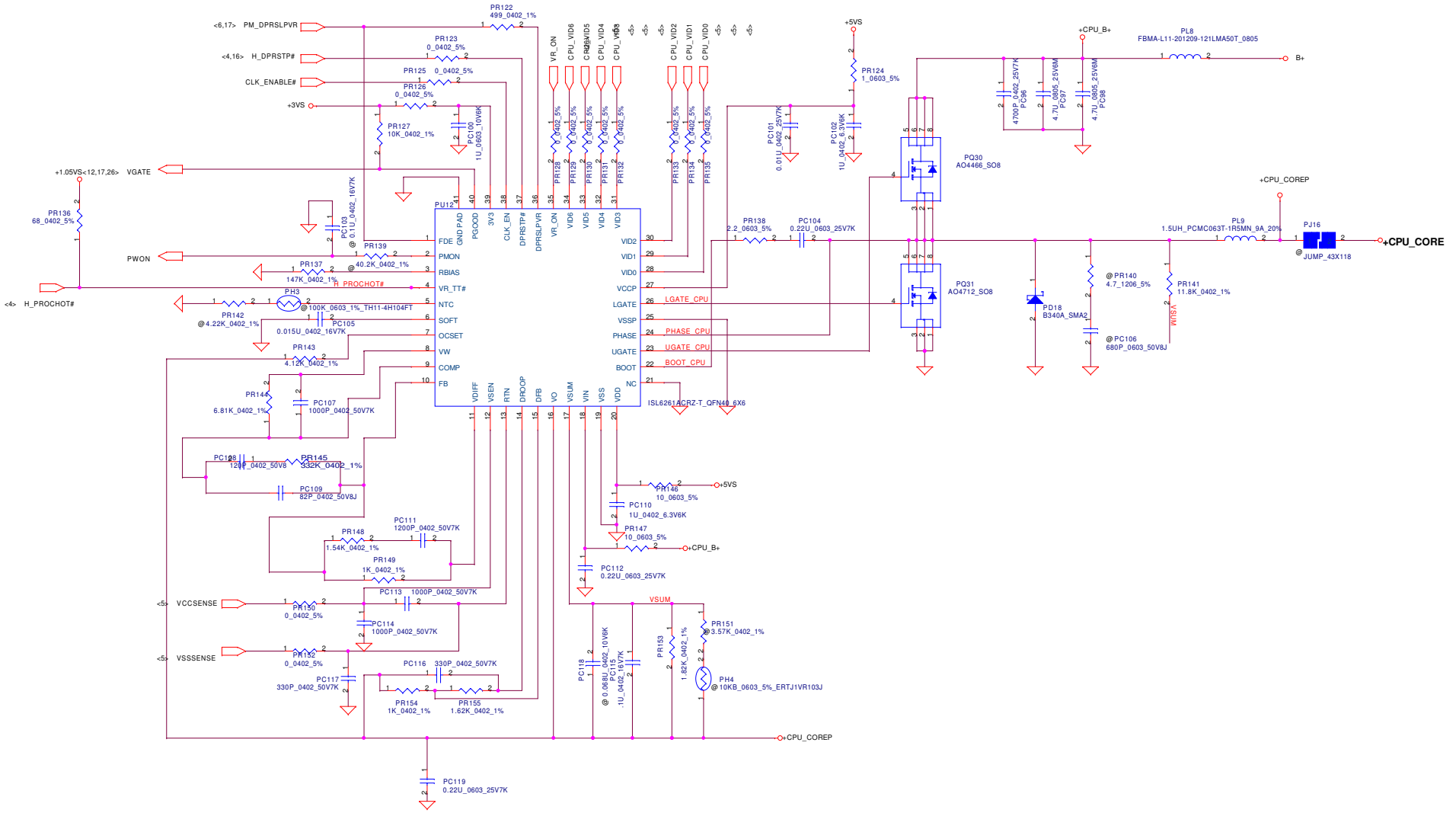
Date: Tuesday, March 10, 2009 | Sheet 35 of 42



Security Classification	Compal Secret Data		
Issued Date	2008/11/17	Deciphered Date	2009/11/17

Compal Electronics, Inc.

Title	+0.9VSP/+1.5VP/+2.5VSP	
Size	Document Number: KAVAA LA-5121P M/B	Rev: 1.0
Date: Tuesday, March 10, 2009	Sheet 36 of 42	



Security Classification	Compal Secret Data		
Issued Date	2008/11/17	Deciphered Date	2009/11/17

Compal Electronics, Inc.

Title: +CPU_CORE

Size	Document Number	Rev
	KAVAA LA-5121P M/B	1.0

Date: Tuesday, March 10, 2009 | Sheet 37 of 42

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
EVT		P34-3VALW/5VALW	Change PD17 SC1SS355010 TO SC100001K00	Choice the same rating
EVT		P35-1.05VSP/1.8VP	Change PR101&109 0_0603_1% to0_0603_5%	Choice the same rating
EVT		P33-CHARGER	Change PR67 22K_0402_5% to 22K_0402_1%	Choice the same rating
EVT		P36-+0.9VSP/+1.5VP/+2.5VSP	Change PC85 1U_0603_6.3V6M TO 1U_0603_10V6M	Choice the same rating
EVT		P36-+0.9VSP/+1.5VP/+2.5VSP	Change PC88 SE076104KM8 to SE076104K80	Choice the same vender
EVT		P37-+CPU_CORE	Change PC115 SE076104KM8 to SE076104K80	Choice the same vender
EVT		P33-CHARGER	Change PR76 SD03430938L to SD034309380	Choice the A51 component
EVT		P34-3VALW/5VALW	Change PC55 & PC60 SGA00001E00 TO SGA00002900	Choice the small size
DVT		P31-DCIN/DECTOR	Change PF1 SP04107P303 TO SP040000P00	Decrease the rating(Memo)
DVT		P37-+CPU_CORE	Change PC116 & PC117 SE074331K00 TO SE074331K80	Choice the pb free material
DVT		P34-3VALW/5VALW	Change PC60 Sga00002900 TO Sga00001e00	Change main source
DVT		P31-DCIN/DECTOR	Change PJP1 4pin to 2pin	change dimation
DVT		P34-3VALW/5VALW	Change PC55	Change the ESR
DVT		P35-1.05VSP/1.8VP	Change PC79 TO SGA00004800	Change the ESR
DVT		P36-+0.9VSP/+1.5VP/+2.5VSP	Add PC123 0.1u	ESD recommend
DVT		P33-CHARGER	Change PR68 154K_0402_1% to 309K_0402_1%	Design change
DVT		All	Sunber All	RF recommend
PVT		P33-CHARGER	add PR12 10K	Design change
PVT		P33-CHARGER	add pc131 & pc124	RF tema require
PVT		P34-3VALW/5VALW	PR83 & PR79 change to 2.2ohm	**EMI** tema require
PVT		P34-3VALW/5VALW	ADD PC129 & PC130	RF tema require
PVT		P35-1.05VSP/1.8VP	PR101 & PR109 chnage to 2.20hm	EMI team require
PVT		P37-+CPU_CORE	PR138 change to 2.2 ohm	EMI tema require
PVT		P35-1.05VSP/1.8VP	ADD PC128 & PC127& PC125 & PC126	RF team require
PVT		P33-CHARGER	add PQ9 &PR51&PQ12&PQ13	Design change
PVT		P33-CHARGER	Change PR74 & Delete PD15	Design change
PVT		P37-+CPU_CORE	PR140 & PC106 reserved	EMI tema require

PIR (Product Improve Record)

KAVAA LA-5121P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
	08/12/15			
(1)		P15	Del C7 with 220U	For layout placement limit
(2)		P16	Change Net name R182.1 from +RTCBATT to +RTCVCC Change Net name R185.1 from +RTCBATT to +RTCVCC Del C210 with 0.1uf	
(3)		P18	Change Net name C244 from +RTCBATT to +RTCVCC	
(4)		P28	Reversal KB Pin define	For KB pin define difference from PCB Foorprint
	08/12/11			
(1)		P25	Change Card Reader Function "3IN1" to "2IN1"	For Cost down
(2)		P26	Link Net name TS_STOP from U29.85 to JTS.4	For Touch Screen
			Link Net name TS_RES from U29.86 to JTS.5	For Touch Screen
	08/12/10			
(1)		P25	Change Card Reader Footprint T-SOL_143-1400303600_21P_NR-T	
(2)		P28	Change KB Matrix from 30 pin to 34 pin	
(3)		P29	Add D40,D41 for Key board F10/F11 function	
	08/12/09			
(1)		P12	Reserve C472~C478 with 47P	for WWLAN request
(2)		P19	Reserve C479~C481 with 47P	for WWLAN request
(3)		P28	Reserve R399,Q32 for test	for cost down plan
	08/12/05			
(1)		P13	Reserve R468,R469 with 680pF	for EMI request
(2)		P20	Reserve L10,L11,L12 Commom choke for EMI request	for EMI request
(3)		P21	Reserve L13,L14 Commom choke for EMI request	for EMI request
(4)		P22	Add PJ19 and link to +5VS	for Cost Down Plan
(5)		P22	Reserve RA31,RA37,CA34,CA42 for EMI request	for EMI request
(6)		P22	Reserve RA4 with 0 ohm for EMI request	for EMI request
(7)		P28	Reserve R396,Q31,C471,D39 for test	for cost down plan
	08/12/04			
(1)		P17	Change BT_RST# from GPIO37/SATA3GP to GPIO21/SATA0GP	for SW recommend
(2)		P17	Link R204.1 to GPIO37/SATA3GP	for SW recommend
(3)		P26	Change package R749 from 0603 to 0402	for layout placement limit
(4)		P13	Change LVDS footprint to "ACES_87213-2000G_20P"	for ME request
(5)		P21	Change TOUCH SCREEN CONN. footprint to "ACES_87213-0600G_6P"	for ME request
	08/12/01			
(1)		13	Change L4,L5 from Bead to 0ohm	
(2)		14	Change R151,R152 from 2.2K to 4.7K	
(3)		14	Change R153,R154 form 2.2k to 4.7K	
(4)		17	Change power sourse +3VALW to +3V_SB	
(5)		18	Add R385 with 0ohm	
(6)		18	Change R226 from STAR@ to @	
(6)		19	Change R229 from WINMAX@ to ALWAY	
(7)		19	Change C265~C270 form GPS@ to 3GGPS@	
(8)		19	Add R378~R381 with 0ohm for touch screen select	
(9)		20	Add D37,D38 ESD diode to USB D+/- port0,2	
(10)		21	Add Touch screen conn.	
(11)		23	Del RA31,RA32 with 0ohm	
(12)		25	Del RC21 with 0ohm	
(13)		25	Del QC1 with 2N7002	
(14)		25	Change net name CR_LED to CR_LED#	
(15)		26	Del ROM Circuit of reserve	
(16)		28	Del R368 with 300ohm	
(17)		28	Add R382~384 with 300ohm	
(18)		29	Change Q14A form SOT363 to SOT23	
(19)		30	Change R355 from 1k to 3.3k	
(20)		30	Change C451 with 0.1uf and link to +3VALW	
(21)		30	Change R353.2 link from +5VALW to +3VALW	
(22)		30	Change Q14B,Q9 form SOT363 to SOT23	

Compal Electronics, Inc.		
Title: ISPD		
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Date: Tuesday, March 10, 2009	Sheet 39 of 42	

PIR (Product Improve Record)

KAVAA LA-5121P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
	08/12/30			
(1)		P30	Mount R361 with 100K ohm	For SUSP pull high
	08/12/26			
NO		PAGE	MODIFICATION LIST	PURPOSE
(1)		P29	Add U1(SA000036K00)forN280 CPU	
	08/12/25			
(1)		P27	Del R398 with 0 ohm and U32.10 link to GND	For customer recommend
(2)		P31	Change H3 link to GNDA	For EMI request
	08/12/24			
NO		PAGE	MODIFICATION LIST	PURPOSE
(1)		P27	Change U32.7 link to +3VS_HDP	
			Change U32.9 no connect	
	08/12/23			
(1)		P16	Add U15A.AF7 and U15A.AE7 link to GND	The unused STAT port RX signals must be properly tied to ground
	08/12/22			
(1)		P15	Change C203.1 Net name from PLTRST#_R to PLTRST#	
(2)		P12	Reserve C868 with 10P	For Custome request
(3)		P13	Reserve C871 with 10P	For Custome request
(4)		P25	Reserve RC21 with 10 ohm and CC16 with 10P	For Custome request
	08/12/21			
(1)		P16	Change C209 Package from 0603 to 0402	For layout pacement limit
(2)		P18	Change C222 Package from 0603 to 0402	For layout pacement limit
			Change C219 Package from 0603 to 0402	For layout pacement limit
(3)		P25	Mount RC20 with 0 ohm	For CLK 48Mhz
	08/12/18			
(1)		P4	Reserve C484~C495 with 180p	For debug
(2)		P6	Add R403~R405 with 1K ohm	For CPU CLK link to NB
(3)		P10	Change package C61,C62,C68,C78,C79 from 0603 to 0402	For layout pacement limit
			Change package C74,C75 from D2 to B2	For layout pacement limit
(4)		p11	Del C124 with 2.2U	
(5)		P12	Del R85,R87,R88,R89,R92,R94,R95,R96,R102,R105,R106,R109	For CPU BSELE0~2 link to CLK Gen
			Change R90,R91 from 33 ohm to 22 ohm	For damping resistor when loading is two device
			Chagne net name FSB to CPU_BSEL1	For CPU link to CLK Gen
			Del R110,R111 with 10K ohm	For UMA platform not need to reserve
(6)		P13	Change Net name R117.1 from +3V_SB to +3VS	For layout pacement
			Change C183 link from GND to +3VS	For layout pacement
			Change JLVDS pin2 from +LEDVDD to +LCDVDD_L	For LCD power consumption
(7)		P14	Change C190~195 to 2.2P	For EMI request
(8)		P15	Change package to 8P4R with 8.2K	For layout pacement limit
			Dell U16,R180,C206	
(9)		P16	Del R190 with 8.2Kohm	For customer request
			Change R189 from 4.7K to 10K ohm	
			Change Net name from IDE_DIORDY to IDE_DIORDY_IRQ	
(10)		P17	Change R216 from 100K to 330K ohm	For ACIN issue
			Add R215,R406,Q31,R408,D43,R409	For leakage current of RSMRST# Circuit
			Add R410,D44	For EC leakage current to SB
(11)		P18	Add R496 with 0.1U	For soft start
(12)		P18	Add L15 with MBK1608121YZF_0603	For Ripple
(13)		P20	Change C455,C458,C222 from D2 to B2 with 220U	For layout placeemnt limit
			Change U21.4 from USB_EN# to USB_CHG_EN#	For customer request
			Add U21.5 link to U29.74	
(14)		P21	Dell Q17 with 2N7002	For cost down
			Change R237.1 from +5VS to +3VS	
			Chagne C294.2 from GND to +3VS	
(15)		P22	Reserve PJ19	
(16)		P24	Dell CL6 with 10U	
			Change UL3 from HD-024A to NS681680	For cost down
(17)		P25	Reserve CC9,CC12,YC1	
			Mount RC19 for 48Mhz	
			Mount RC20 For 48Mhz	
(18)		P26	Del R304 with 10K ohm	
			Change R307 from 100K to 330K ohm	
			R243 please close to EC	
			Add Net Name USB_CHG_EN#	
			Del D22,R310,R311	
(19)		P27	Change U31 P/N from SA000030500 to SA000035U00	
(20)		P28	Chagne U36 ROM Size from 16M*1 to 8M*1	
			JBK KB Matrix the same to KSKAA	
			Del JP2	
(21)		P29	Change R370,R371,R372,R375,R383,R384,R374,R333 from 120 ohm to 220 ohm	
			Del R325,R326	
(22)		p30	Add R401,R402 with 10K ohm	

Security Classification	Compal Secret Data		
Issued Date	2008/11/17	Deciphered Date	2009/11/17

Compal Electronics, Inc.		
Title	ISPD	
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PIR (Product Improve Record)

KAVAA LA-5121P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1-->0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1)	1/13	10	Change D1 to CH751H-40PT_SOD323-2	For BOM simplify
2)	1/13	18	Change D7,D8 to CH751H-40PT_SOD323-2	For BOM simplify
3)	1/13	23	Change net name from JLINE to JEXMIC	For EXMIC JACK
4)	1/13	23	Change net name from JEXMIC to JLINE	For JLINE JACK
5)	1/13	29	Chagne JPOWER.3 net name from ON/OFFBTN# to ON/OFFBTN#_R	For PWR/B can't power on with battery mode
	1/13	30	Add H20,H21	For half card
6)	1/22	13	Change R117 from 47k to 100K ohm	For LCD Soft start reduse inrush current
			Change Q11 from SI2301BDS to A03413	For LCD Soft start reduse inrush current
			Add C498 with 0.01uF	For LCD Soft start reduse inrush current
7)	1/22	19	Change SW1.3 to dummy pin	For Kill switch issue
			Change SW1.1 to GND	For Kill switch issue
8)	1/22	21	Change R238 from 10K to 47K	For BT Soft start reduse inrush current
			Add C499 with 0.01uF	For BT Soft start reduse inrush current
9)	1/22	22	Del Net name AMP_SPK_R and AMP_SPK_L	For Mono SPK
			Add Net name AMP_SPK from UA2.37 to UA3.17	For Mono SPK
		23	Del CA32 with 0.033UF	For Codec output less than 0.9V
			Add RA38,RA40 with 1K ohm	For Codec output less than 0.9V
			Add RA39,RA41 with 9.09k ohm	For Codec output less than 0.9V
			Add CA43 with 1uf	For Codec output less than 0.9V
	1/22	27	Change U34 P/N from SA00000XZ50 to SA000037Y60	For G-sensor controller chip change
		29	JTOUCH pin define reversal	For ME request assembly easy
		30	Change R355 from 3.3K to 47K	For LAN Soft start reduse inrush current
			Add C500 with 0.01uf	For LAN Soft start reduse inrush current
10)	2/3	14	Reserve C504 with 0.1uf	For EMI request
	2/3	19	Add R411 with 0 ohm	Del Kill switch function
	2/3		Reserve SW1,RM1,U17,C264 for del kill switch function	Del kill switch function
	2/3	20	Change D15,D38,D37 from PRTR5V0U2X to CM1293A-04SO	For EMI request
	2/3	23	Change DA3,DA6,DA7 from PJDLC05 to PACDN042Y3R	For EMI request
	2/3	28	Add C501,C502 with 330pf	For EMI request
			Add C503 with 470pf	For EMI request
			Add R412 with 10 ohm	For EMI request
			Add C508 with 6pf	For EMI request
	2/3	29	Add R413,R414,R415 with 0 ohm	For EMI request
			Reserve C505,C506,C507 with 0.1uf	For EMI request
			Change D27 from PJDLC05 to PACDN042Y3R	For EMI request
			Del D25 with PJDLC05	For EMI request
			Change R375 from 220 to 300 ohm	For White LED of PWR/B
			Change R375.1 Net name from +3VALW to +5VALW	For White LED of PWR/B
11)	2/4	22	Change CA14 from 100pf to 0.1uf	For SPK noise issue
			Add PJ20,PJ21	For customer request(Echo Peak Issue)
		24	Change UL3 from 16pin(SP050003N00) to 24pin(SP050003P00)	For EMI issue
12)	2/5	06	Add R416 with 0 ohm	For WWLAN request
			Reserve C511 with 22pf	For WWLAN request
		12	Reserve C509,C510 with 10p	For WWLAN request
		22	Reserve UA1,CA9,CA11	For cost down plan
	2/6		Modify JUSBA,JUSBB,JUSBC Symbol for GND pad	For GND pin
		10	Reserve C67 with 220uF	For Cost down plan
			Add C514 with 0.1uF	For ESD team request
		23	Change RA38,RA40 with 2K ohm	For Codec output less than 0.9V
			Change RA39,RA41 with 8.2K ohm	For Codec output less than 0.9V
		24	Change UL3 from NS681680(SP050003N00)to 8456E(SP050005V00)	For ESD fail issue
		30	Reserve +1.5VS,+1.05VS,+0.9VS,+1.8VS discharge circuit	For Cost down plan
		27	Reserve C867 with 0.22uf	For U33.4 NC pin
			Change U33 from APL5151-33BC to G9191-330T1U	For power sequence issues on HPC
	2/9	20	Change C455,C288 from 220uf to 150uf	
			Reserve C458 with 150uf	For Cost down plan
	2/11	22	Mount RA13 with 0 ohm	For EMI requet open channel
		27	Change U31 from SA000035U00 to SA000039900	For Customer request version change
	2/16	14	Mount C504 with 0.1uF	For EMI request
		23	Mount DA3/DA6 with PACDN042Y3R	For EMI request
		17	Reserve C217,C218 with 0.1uF	For Reserve WWAN PCIE interface

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NO	DATE	PAGE	MODIFICATION LIST		PURPOSE
1)	2/25	4	Mount	C484~C495 with 220pF	For EMI request
2)	2/25	6	Change	Net name from ICH_POK to ICH_PWROK	For correcting power down sequence
3)	2/25	12	Change	R81,R82 from 0 ohm to FBMH1608HM601-T_0603	For WWAN request
			Mount	C133,C141 with 47pF	For WWAN request
			Mount	C142,C143,C144,C145,C146,C868 with 22pF	For WWAN request
4)	2/25	13	Mount	C871 with 10pF	For WWAN request
5)	2/25	15	Mount	C203,C204 with 0.1uF	For WWAN request
6)	2/25	17	Change	Net name from ICH_POK to ICH_PWROK	For correcting power down sequence
			Add	R418 with 10K ohm	For correcting power down sequence
			Add	U37 with TC7SHO8FUF_SSOP5(SA007080100)	For correcting power down sequence
			Reserve	R417 with 0 ohm	For correcting power down sequence
7)	2/25	19	Mount	C479,C480,C481,C482 with 47pF	For WWAN request
8)	2/25	22	Mount	RA31 with 22 ohm,CA34 with 10pF	For WWAN request
9)	2/25	23	Change	JEXMIC,JLINE PCB footprint to JA6033L-B3T4-7F_6P-T	For ME request
10)	2/25	25	Mount	CC16 with 10pf,RC21 with 10 ohm	For WWAN request
11)	2/25	26	Change	U29.104 net name from ICH_POK to EC_PWROK	For correcting power down sequence
12)	2/25	28	Mount	C508 with 33pF,R412 with 33 ohm	For WWAN request
13)	2/25	30	Reserve	R349 with 200K ohm	For design change
			Change	C447 from 0.01uf to 0.022uF	For design change
			Change	R346 from 20K to 47K ohm	For design change
14)	3/2	14	Change	D5 from SC1B491D000 to SCS00002000	For buyer recommend
		28	Change	Change U36 to MX25L8005M2C(SA00000XT00)	For CLK frequency 75MHz
	3/2	30	Change	H18 from H_3P0N to H_2P6N	For ME request
				H19 from H_6P0X3P0N to H_6P0X2P6N	For ME reqeust
	3/4	08	Add	GMCH_INVT_PWM on U3.H30	For support DPST function
		13	Add	R419 with 0 ohm	For support DPST function
			Reserve	R420 with 0 ohm	For support DPST function
			Del	JLVDS pin 2 for dummy pin	For prevent short B+
		23	Mount	DA5 with PJDLC05	For EMI request
		23	Reserve	DA6 with PJDLC05	For EMI reqeust
		20	Add	C515,C516 with 470pF	For EMI request
		28	Mount	C414~C437,C461 with 100pF	For EMI request
		17	Add	R421 with 330K ohm to +3VALW	For USB over current protect
		17	Add	D45 with CH751H-40PT to USB_OC#0_2	For USB over current protect
		17	Change	RP7.4 from USB_OC#0_2 to USB_OC#0_2_D	For USB over current protect
		17	Change	U15.D3 from USB_OC#0_2 to USB_OC#0_2_D	For USB over current protect
		26	Add	Net name to USB_OC#0_2	For USB over current protect
		29	Change	R413,R414,R415 from 0 ohm to FBMA-10-100505-151T	For EMI request
		30	Add	C517~C520 with 0.1uF	For ESD request
	3/5	12	Reserve	R427 with 0 ohm	For Silego source chip
			Add	R428 with 10K ohm to +3VS	For Silego source chip
			Change	U4.54 from H_STP_PCI# to H_STP_PCI#_R	For Silego source chip
	3/5	17	Add	R423,R424 with 0 ohm	For design change
			Reserve	R410,R421 with 330 K ohm	For design change
			Reserve	D44,D45 with CH751H-40PT	For design change
		19	Add	R425,R426 with 0 ohm	For debug
		30	Reserve	R422 with 0 ohm and PJ22 with JUMP_43X79	For EMI request
		30	Change	H15 to Non-PTH hole	For design change
	3/10	17	Change	R214.2,U15.F20 from ICH_PCIE_WAKE# to EC_SWI#	For wakeup LAN function
		30	Add	EC_SWI# and link to both U29.103 to U15.F20	For wakeup LAN function
	3/10	22	Change	CA18 from 10uF to 0.1uF	For Audio noise

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